

A Ring Temperature Sensor for Quantum Applications

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Abstract—In this paper, we present a fully integrated ring-oscillator (RO)-based temperature sensor for quantum computing applications. As the quantum states exhibit an exponential sensitivity to the on-die cryogenic temperature change, any such temperature variation due to, for example, local heating islands arising from the poor thermal conductivity of silicon should be monitored. For this purpose, we exploit a compact RO sensor placed in the vicinity of qubits. The proposed approach employs four differently sized oscillators and two V_{BG} s to generate, in total, eight different temperature-dependent oscillating frequency signals. Then, by performing their polynomial fitting, a linear temperature-frequency compensating model for the proposed sensor is derived. Fabricated in 22 nm FD-SOI technology, the proposed sensor occupies 0.0016 mm^2 , consumes $128 \mu\text{W}$ and achieves maximum inaccuracy of $\pm 2.1 \text{ K}$ in a wide temperature range from 3 to 270 K.

Index Terms—Cryo-CMOS, qubits, quantum computer, ring oscillator (RO), phase noise (PN), temperature sensor, back-gate voltage, fully depleted silicon-on-insulator (FD-SOI).

I. INTRODUCTION

Semiconductor qubits offer a promise of full quantum system-on-chip (SoC) integration and mass scalability but they are extremely fragile and must operate under extremely low cryogenic temperatures of $\leq 4 \text{ K}$ in order to preserve their coherent superposition state [1].

Fig. 1 illustrates a quantum processor that operates at $\sim 4 \text{ K}$ and is fully integrated with its interface electronics in a 22-nm fully depleted silicon-on-insulator (FD-SOI) CMOS process [2], [3]. In contrast to bulk CMOS, FD-SOI provides a thin semiconductor layer isolated from the substrate by a 20-nm buried oxide (BOX) layer. Therefore, a quantum particle can be strictly confined inside the 5-nm thin semiconductor film where it can be controlled accurately, while being isolated from the substrate impurities to further increase its decoherence time. The qubits, as well as the nearby single-electron drivers and detectors need to be fully operational at $\sim 4 \text{ K}$. The silicon material in general, but the FD-SOI stack in particular, is a poor thermal conductor at cryo temperatures [4]. As a result, it is necessary to monitor for any possible hot-spot islands on the die by multiple temperature sensors placed close to the qubits and also distributed all over the die rather than being implemented outside the die, as an off-chip temperature sensor.

Several types of silicon-based temperature sensors have been reported for general-purpose applications but nothing specifically for deep cryo temperatures. BJT and resistor based temperature sensors have high resolution and accuracy [5], [6] but they suffer from the need for high-resolution and power-hungry ADCs. Parasitic substrate pnp BJTs are usually employed in bandgap references and temperature sensors, but

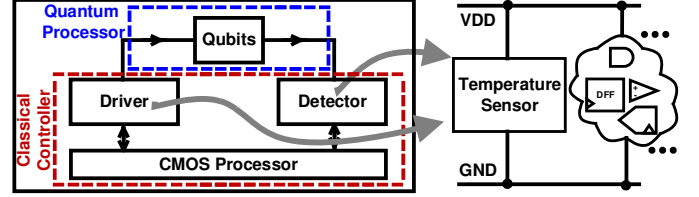


Fig. 1. Example of temperature sensor units integrated on-chip within a quantum system-on-chip (SoC) processor.

their behavior deteriorates below 70 K due to the freeze-out in the base [7]. Thermal-diffusivity (TD) based sensors can achieve high accuracy [8] but they heat up the die and still require a high resolution ADC. MOSFET-based sensors usually use two signals that are proportional/complementary to the temperature to modulate the output frequency of a VCO [9], [10]. However, in many modern processes, thin-oxide devices with a proportional/complementary relationship with the temperature are not offered. An alternative method in MOSFET-based sensors was introduced in [11] to exploit the temperature-frequency dependency of ring-oscillators to convert the temperature into the clocking frequency.

Inverter ring-oscillator (RO) based temperature sensors are particularly attractive in our application since they can reliably work down to the deep cryogenic temperatures [7], can be very compact, therefore placed in the vicinity of qubits and other critical electronic circuits so as to improve the temperature estimation. In this letter, a new method of low hardware complexity is proposed to measure local on-die temperature of cryo-CMOS circuits. For this purpose, we make use of the back-gate body biasing voltages (V_{BG}) in four differently sized inverter-based ROs. The output frequency of each RO is dependent on V_{BG} , inverter sizes and operating temperature. By developing a mathematical approximation frequency-temperature model, considering the physical and electrical features of the ROs, such as their sizes or the V_{BG} , the on-chip temperature can be conveniently estimated.

II. PROPOSED ON-CHIP TEMPERATURE SENSOR

It is well known that the temperature sensitivity of an RO can be tuned by changing its supply voltage V_{DD} or threshold voltage V_t of its transistors. Since providing a variable V_{DD} for the RO would be costly, adjusting V_t appears more convenient [11]. The FD-SOI technology facilitates effective access to the V_{BG} of transistors for the purpose of adjusting V_t .

Fig. 2 illustrates the proposed concept. The RO's oscillating frequency (f_{osc}) increases with the lowering of temperature due to the increased carrier mobility, but this is against the simultaneous increase in V_t . Hence, the largely expected inverse relationship between the RO frequency and

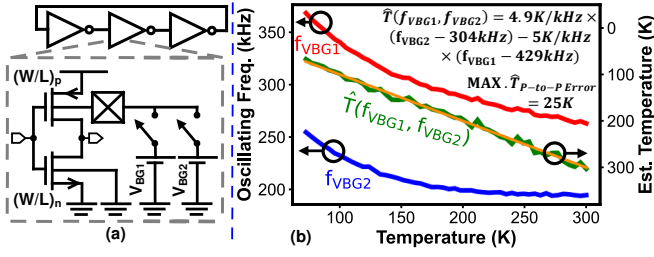


Fig. 2. Operating principle of the proposed temperature sensor: (a) schematic, (b) Cadence simulated RO's frequency vs. temperature for different PMOS V_{BG} s and a linear combination $\hat{T}(f_{VBG1}, f_{VBG2})$ thereof

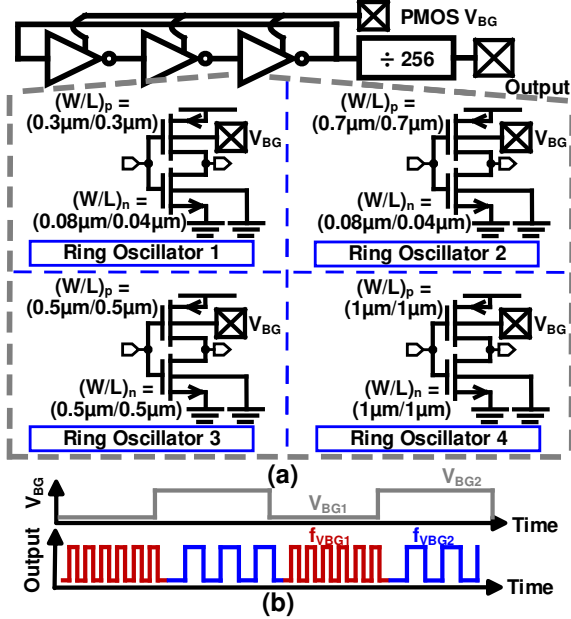


Fig. 3. (a) Architecture of the proposed temperature sensor with schematics of the four differently sized inverters. (b) Example waveform during the system operation.

temperature will exhibit substantial nonlinearity. Fortunately, the nonlinearity can be reduced by appropriately combining *multiple* of such characteristics at different V_i 's. Fig. 2(b) plots two simulated f -vs.- T characteristics for $V_{BG1} = 0$ and $V_{BG2} = 1.8V$ for an RO consisting of 31 inverters with $(W/L)_{pmos}$ and $(W/L)_{nmos}$ equal to $(0.3\mu m/0.3\mu m)$ and $(0.08\mu m/0.04\mu m)$, respectively. The estimated absolute temperature $\hat{T}(f_{VBG1}, f_{VBG2})$ is derived by an appropriate linear combination of the curves. Yet, for better linearity, we can extend the concept to a higher number of ROs (four in this work), each with a different size (area) of transistors.

Fig. 3(a) shows the transistor sizing of the four independent ROs implemented in the proposed temperature sensor. The sizes are varied from small-area MOSFETs to large ones in order to increase the overall sensor's accuracy. V_{BG} of the NMOS FETs is grounded while V_{BG} of the PMOS FETs is connected here to a programmable off-chip supply voltage source. The fabricated sample chip is mounted on a printed circuit board (PCB) located inside a cryo chamber [shown later in Fig. 6(b)], resulting in a long distance and heavy impedance load from the cryo chamber to the off-chip frequency counter

(the counters could be easily integrated as in [11]). In order to efficiently read the RO frequencies, eight stages of cascaded $\div 2$ dividers are inserted before the output pad.

Fig. 3(b) illustrates the timing diagram of the PMOS V_{BG} stimulus and the corresponding output clock of the proposed temperature sensor. By continuously switching the PMOS's V_{BG} between V_{BG1} and V_{BG2} , the RO frequency changes between f_{BG1} and f_{BG2} . By appropriately combining different clocking frequencies of four differently sized ROs and also with two different PMOS body-biasing voltages (i.e. V_{BG1} and V_{BG2}), yielding a total of $N = 8$ different clocking frequencies over different temperatures (i.e. f_1, \dots, f_N), a linear relationship between the combined RO frequencies and the actual temperature of the system can be derived. In the implemented system, the clocking frequency of each of the four ROs, along with their frequency changes due to the V_{BG} switching, are read with off-chip counters and then processed.

As previously emphasized in Fig. 2(b), the raw frequency-to-temperature mapping in the implemented ROs exhibits significant non-linear components. Nevertheless, by using a simplified Koopman approach [12], which is normally applied to a non-linear system to model it as a linear operator by increasing their modeling dimensions, here we can find a linear operator of the frequency-temperature characteristic such that the temperature estimation error would be minimized. To illustrate this idea, let us assume that each of the $N = 8$ measured RO frequencies (i.e. f_1, \dots, f_N) allows a polynomial approximation of the eighth order:

$$\begin{bmatrix} f_1(T) \\ \vdots \\ f_N(T) \end{bmatrix} = \begin{bmatrix} A_{1,1} & \dots & A_{1,N} \\ \vdots & & \vdots \\ A_{N,1} & \dots & A_{N,N} \end{bmatrix} \times \begin{bmatrix} T^1 \\ \vdots \\ T^N \end{bmatrix} + \begin{bmatrix} f_1^* \\ \vdots \\ f_N^* \end{bmatrix} \quad (1)$$

where T^i is the actual temperature of the environment raised to the power of i ($= 1, 2, \dots, N$) that defines the order of the polynomial approximation equation; f_i^* and $A_{i,j}$ are the DC and non-DC approximation coefficients, respectively, which can be found by polynomial fitting methods. By considering the inverse of $A_{i,j}$ (i.e. $A_{i,j}^{-1}$) to be $a_{i,j}$, the approximated model of the frequency-temperature (i.e. \hat{T}^i) can be estimated as:

$$\begin{bmatrix} \hat{T}^1(f_1, \dots, f_N) \\ \vdots \\ \hat{T}^N(f_1, \dots, f_N) \end{bmatrix} = \begin{bmatrix} a_{1,1} & \dots & a_{1,N} \\ \vdots & & \vdots \\ a_{N,1} & \dots & a_{N,N} \end{bmatrix} \times \begin{bmatrix} f_1 - f_1^* \\ \vdots \\ f_N - f_N^* \end{bmatrix} \quad (2)$$

The first term $\hat{T}^1(f_1, \dots, f_N)$ in expression (2) defines the linear approximation of the temperature dependence:

$$\hat{T}(f_1, \dots, f_8) \equiv \hat{T}^1(f_1, \dots, f_8) = \sum_{i=1}^8 a_{1,i}(f_i - f_i^*) \quad (3)$$

In summary, utilizing the measured output clocking frequency of the four differently sized ROs with respect to the temperature and V_{BG} variations, coefficients a_i and f_i^* in (3) can be readily estimated using off-chip post-processing polynomial fitting. In future implementations, the counters and the calculation logic could be conveniently implemented on-chip.

III. MONTE CARLO SIMULATION RESULTS

To verify the efficacy of the proposed temperature sensor, we first present the circuit-level simulation results. The four independent ROs of Fig.3 are simulated in Cadence based on the PDK of the used 22 nm FD-SOI technology. The four ROs are connected independently to the 0.8 V supply voltage and their output free-running oscillation frequencies, for two different V_{BG} s (i.e. 0 and 1.8 V) are measured. All the simulation measurement steps were repeated for 100 Monte Carlo trials.

Fig. 4(a)–(d) plot their f_{osc} s from 300 K (room temperature, RT) down to 203 K for two different V_{BG} s. We note that the vendor’s PDK supports the temperatures down to 70 K, but the model accuracy is known to be substantially degraded up until 203 K [13]. For $V_{BG} = 0$ V, the f_{osc} range is between 331 to 232 kHz, 163 to 115 kHz, 156 to 104 kHz and 49 to 33 kHz for RO 1 to 4, respectively. For $V_{BG} = 1.8$ V, the f_{osc} range is between 241 to 167 kHz, 122 to 87 kHz, 112 to 76 kHz and 37 to 21 kHz for RO 1 to 4 respectively. Each line represents one Monte-Carlo simulation trial. All Monte Carlo simulation results were applied to the mathematical procedure explained in Section II and, for each of the 100 trials, one set of temperature errors between the actual temperature and estimated temperature was calculated. From (3) and by performing polynomial fitting of the measured RO output, f_i , $a_{1,i}$ and f_i^* were estimated. Fig. 4(e) shows the temperature error for all the 100 Monte Carlo trials over temperature.

The maximum peak-to-peak temperature estimation error for all trials (i.e., ΔT_{pp}) is ± 0.5 K. Fig. 4(f) shows the probability density function (PDF) of the estimated error of the simulated system. The standard deviation (STD) of the calculated temperature error is estimated at 0.1 K. The maximum temperature error (i.e., ΔT_{pp}) is estimated at 0.5 K, which is smaller than the measurement results later presented in Section IV (i.e. 2.1 K). The increase in the measured maximum error is attributed to the expected inaccuracy of the PDK simulation results at deep cryogenic temperatures, but also to the possible injection of extra noise from the supply voltage in the cryo chamber into the sensors during the measurement.

IV. EXPERIMENTAL RESULTS

The proposed RO-based temperature sensor is part of a quantum SoC implemented in 22-nm FD-SOI CMOS. Fig. 6(a) shows a zoomed-in portion of the chip micrograph that indicates the locations and layout of the four constituent ROs with their clock dividers for external measurement. The implemented ROs #1, 2, 3, 4 occupy 17.9×18.6 , 17.7×22.0 , 16.9×22.6 and $21.3 \times 25.6 \mu\text{m}^2$, respectively, including the clock dividers. They respectively consume 128, 84, 90 and $52.4 \mu\text{W}$ at cryo and 94.7, 58.14, 55.9 and $33.6 \mu\text{W}$ at RT. Fig. 6(b) illustrates the cryo chamber which cools down the SoC to <3.8 K. A CTC100 industrial cryo temperature sensor is placed within 2 mm of the SoC to measure its temperature environment with 0.1 K accuracy. By turning off the helium gas compressor when its temperature is stabilized at <3.8 K,

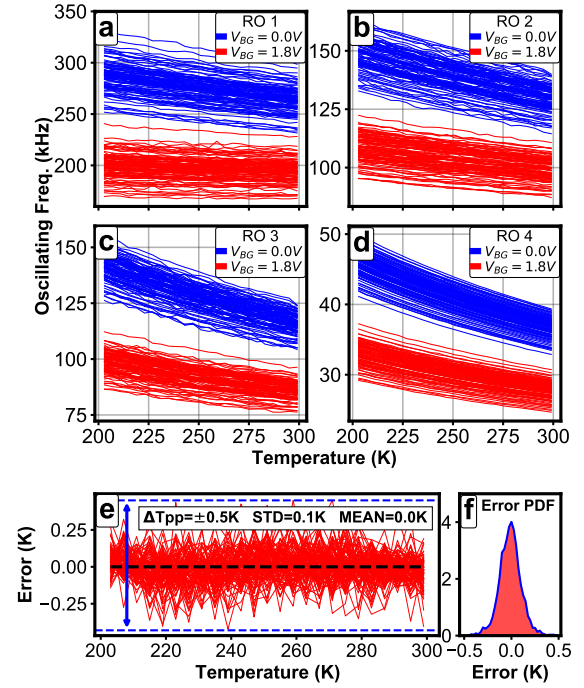


Fig. 4. Monte Carlo simulation results of the proposed system: (a) f_{osc} of RO#1 (a), RO#2 (b), RO#3 (c), RO#4 (d) over temperature for two different V_{BG} s. (e) Resulting temperature simulation error. (f) PDF of the calculated temperature error.

the chamber temperature will gradually increase. During this slow process, the ROs are characterized at each temperature point.

Fig. 5 shows the measured phase noise (PN) versus frequency offset at both the room and cryo temperatures for the four ROs when V_{BG} is 0 V. The integrated jitter noise between 2 kHz to 40 kHz is measured at 3.41/1.37 nsec for RO#1, 2.78/1.11 nsec for RO#2, 3.06/1.53 nsec for RO#3, and 4.13/3.28 nsec for RO#4, at cryo/RT, respectively. The maximum RO frequency is 379 kHz (RO#1). Considering that the fastest RO needs to oscillate in the worst-case scenario for 100 cycles before estimating its frequency, as well as 3σ of the the maximum jitter (i.e. $\sigma_{max} = 4.13$ nsec) injected (RO#4, the slowest), this results in the maximum time error of $100 \times 3 \times 4.13 \text{ nsec} = 1.23 \mu\text{sec}$, which is still less than one RO period, i.e. $2.63 \mu\text{sec}$. This calculation underscores the destructive effect of flicker PN on the intended operation, which is getting much worse at cryo (also observed in [14]).

Fig. 7 illustrates the measured flicker-dominated PN at 1 kHz for different V_{BG} at cryo (3.7 K) and room (290 K) temperatures. The effect of V_{BG} on PN varies over temperature. As an example, in RO#1, increasing V_{BG} at cryo results in the reduction of flicker PN, while this trend is reversed at RT for this RO. Measured PN of RO#2 stays almost the same at different V_{BG} . Based on [15], asymmetry of the rising and falling edges of the RO’s output signals results in the increase of the impulse sensitivity function (ISF) of the RO which eventually leads to the increase of PN. The effects of V_{BG} adjustment on the oscillator PN require more research and thus is beyond the scope of this paper.

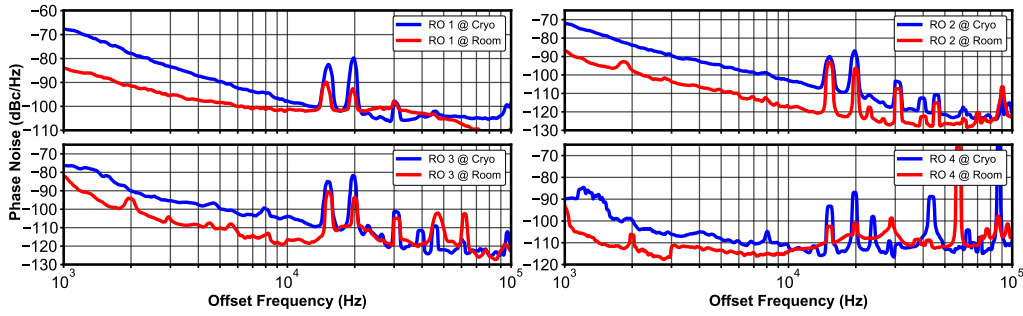


Fig. 5. Measured PN vs. offset frequency at RT and cryo Temp. for the four ROs when $V_{BG} = 0$ V.

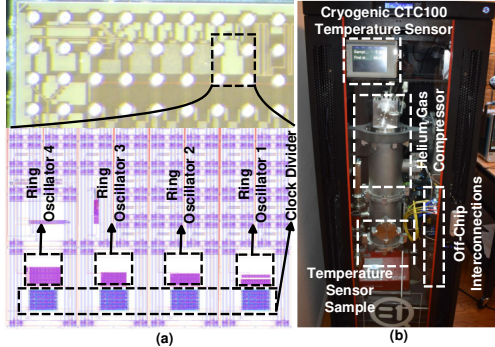


Fig. 6. (a) Die micrograph and zoomed portion of the proposed Temp. sensor. The ball pad separation is 0.25 mm^2 . (b) Test setup for the proposed Temp. sensor housed in a standard 18-inch rack.

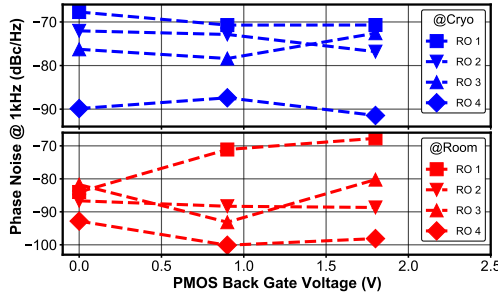


Fig. 7. Measured PN vs. PMOS back gate voltage for different ROs at RT and cryo Temp.

The integrated PN between 2 kHz to 40 kHz is measured as -44.8 and -53.1 dBc for RO 1, -51.4 and -61 dBc for RO 2, -50 and -58.7 dBc for RO 3, -55.9 and -61.5 dBc for RO 4, at cryo and RT, respectively.

Fig. 8(a) shows the measured f_{osc} f_1, \dots, f_8 of the four constituting ROs with two different V_{BG} levels. $f_{1,3,5,7}$ are the output frequencies of the ROs #1..#4, respectively, when $V_{BG} = 0$ V, while $f_{2,4,6,8}$ correspond to $V_{BG} = 1.8$ V. The f_i -vs.- T curves exhibit highly non-linear and rather unpredictable behavior. From (3) and by performing off-chip polynomial fitting of the measured RO output f_i frequencies, $a_{1,i}$ can be estimated as $(-4.5, 1.7, -7.6, -12.4, -4.1, 11.8, 72.9, -41.5)$ K/kHz and f_i^* as $(233, 382.3, 133.8, 219, 139.7, 231.7, 50.6, 87.1)$ kHz. As shown in Fig. 8(b), with thus calculated coefficients, the estimated frequency-temperature model in (3), (i.e. $\hat{T}(f_1, f_2, \dots, f_8)$), is well matched with the actual temperature, with the maximum peak-to-peak temperature estimation error (i.e., ΔT_{pp}) of ± 2.1 K, as illustrated in Fig. 8(c).

Performance summary and comparison with prior art is

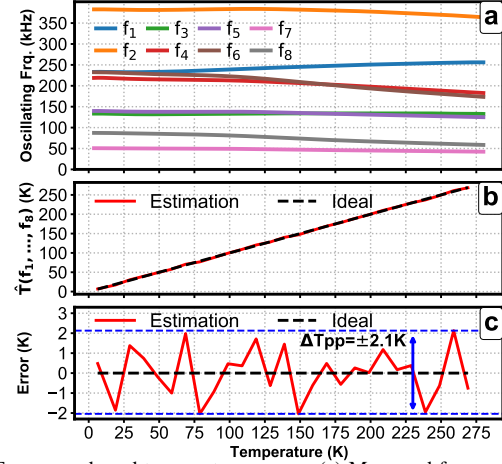


Fig. 8. Frequency-based temperature sensor: (a) Measured frequencies of the eight ROs; (b) Temperature estimator \hat{T} as the best-fit linear combination of all eight frequencies; (c) Resulting temperature measurement error.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART.

| Reference | [8] | [9] | [10] | [11] | This Work |
|------------------------|---------|---------|---------|---------|-----------|
| Process (nm) | 180 | 55 | 130 | 65 | 22 |
| Type | TD | MOS | MOS | MOS | MOS |
| Temp. Range [K] | 258-378 | 233-358 | 273-353 | 273-373 | 3-270 |
| Inaccuracy [K] | 0.2 | 0.25 | 0.44 | 0.9 | 2.1 |
| Power [μ W] | 5100 | 0.86 | 0.2 | 154 | 128 |
| Area [mm^2] | 0.2 | 0.002 | 0.07 | 0.004 | 0.0016 |

presented in Table I. The proposed sensor is the first ever report of a CMOS temperature sensor over a wide range of temperatures from the deep cryo to RT.

V. CONCLUSION

This letter demonstrates an inverter-based RO temperature sensor suitable for supporting quantum computing applications. The proposed sensor can be placed very close to the quantum core to monitor the formation of hot-spot islands on the die due to the deleterious effects of poor thermal conductivity of silicon at cryo. The measured non-linear frequency-vs.-temperature characteristics of four diverse ROs were linearized using the Koopman approach, resulting in the maximum peak-to-peak temperature estimation error of ± 2.1 K. We also confirmed through PN measurements that the expected increase of RO jitter at cryo will not affect the measured frequency-temperature output model of the ROs.

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