Silicon spin qubits: A scalable solution for quantum computing

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***Abstract*—Quantum computers promise to revolutionize information processing, offering game-changing opportunities in fields such as cryptography, machine learning, drug discovery, etc. However, building large-scale quantum computers presents significant challenges, requiring both fundamental research and technological breakthroughs. Among the various platforms proposed for the realization of the core of the quantum hardware, qubits realized in semiconductor nanostructures stand out. One of their key advantages lies in their compatibility with standard semiconductor manufacturing, enabling, among other capabilities, their co-integration with control and readout electronics, thus improving scalability and reducing interconnect complexity. In this review, we discuss recent advances in silicon-based spin qubits and present an overview of the progress and challenges in developing large-scale quantum computing systems based on this architecture.**

***Index Terms*—quantum computers, quantum information, silicon qubits, cryogenic electronics, quantum-classical interface**

I. INTRODUCTION

By leveraging the principles of quantum mechanics to process information, quantum computers promise to revolutionize several scientific and technological fields, such as cryptography [1], machine learning, artificial intelligence [2], drug design and discovery [3], medicine development [4], and energy consumption [5]. Unlike their classical counterpart, quantum computers can offer an exponential improvement in calculation times and promise to solve computational problems considered notoriously difficult even for the most powerful supercomputers today [6], [7].

Building a full-fledged large-scale quantum computer, however, presents significant challenges. Such an endeavor requires a combination of groundbreaking research and new technological breakthroughs. The building block of a quantum computer is the quantum bit, or qubit, which serves to encode and process quantum information. Various technological platforms have been proposed for qubit implementation, including superconducting circuits [8], trapped ions [9], optical lattices [10], nitrogen-vacancy (NV) centers in diamond [11], and many more.

Among these approaches, spin qubits in silicon nanostructrures stand out as one of the most promising candidate technologies due to their compatibility with the industry-standard semiconductor manufacturing methods [12]. This allows for the fabrication of thousands of qubits on the same chip and their co-integration with control and readout electronics, which are primarily located away from the qubits and typically operate at room temperature, in contrast to the qubits, which require cryogenic temperatures [13]. A single chip integration would be a critical step towards large-scale quantum computers and could drastically reduce overhead, and interconnect complexity, which is the main bottleneck for many other qubit platforms [14], [15]. Nevertheless, achieving reliable and compact control systems functional at cryogenic temperatures, required for quantum computation operations, and are coupled to the quantum processor remains a challenge [16].

As silicon spin qubits advance rapidly with yearly improvements in performance and significant experimental and theoretical progress, we present in this review a brief, up-to-date overview of recent developments in silicon electron spin qubits, focusing on their technological implementation and potential for scalability [17], while highlighting key research areas. We start by discussing two of the main proposed architectures to process quantum information using the electronic or nuclear spin states, i.e. dopant-atom spin qubits and quantum-dot spin qubits. We outline the key characteristics of each approach and discuss recent advancements. We then review state-of-the-art implementations for each approach, as well as the obstacles on the way towards large-scale quantum information processing. Next, we present advances in monolithic co-integration of qubits with electronic circuits designed for initialization, control and readout. We conclude with a brief summary of key open questions and an overview of the global industrial landscape, highlighting the growing interest in commercializing these technologies.

II. SEMICONDUCTOR SPIN QUBITS

The spin qubit architecture was initially introduced in 1998 through two seminal papers proposing two different approaches. The first approach relies on encoding quantum information in the spin states of electrons confined in quantum dots hosted in semiconductor nanostructures [18]. The second approach involves encoding quantum information in the spin states of electrons or nuclei of dopant atoms introduced into semiconductor devices. In both architectures, quantum computation is achieved by selectively addressing and manipulating individual spins [19].

A. *Donor-based spin qubits*

In Kane's proposal, quantum information is encoded in the nuclear spins of phosphorus-31 (^{31}P) donor atoms injected in crystalline silicon (Fig. 1). Phosphorus atoms possess a single loosely bound electron when coupled to the silicon lattice, allowing the use of both the electron and nuclear spin of the ^{31}P to create a qubit. A 3D isotropic confinement is thus formed, similar to that of an atomic system. Significant progress in implementing such a device and performance has been made since then, thanks in large part to the remarkable advances in modern semiconductor manufacturing over the last decades, which have enabled the fabrication and manipulation of atomic-scale structures [20].

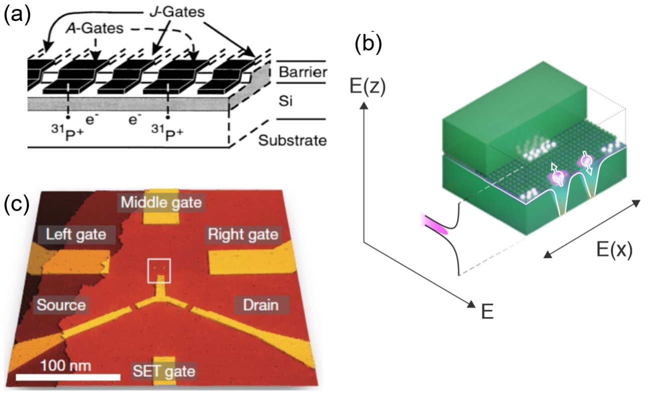

Fig. 1. Donor-based spin qubits in silicon (a) Schematic of Kane's original donor qubit proposal illustrating a linear array of ^{31}P donors in a silicon host structure [19] (b) Device schematic with corresponding energy diagram, showing 3D confinement achieved by the positive potential of the donor atom. Figure adapted from [17]. (c) Donor qubit device with demonstrated two-qubit gate operations [21]

B. *Electrostatically gate-defined quantum dot spin qubits*

In Loss and DiVincenzo's proposal, quantum information is encoded in the spin states of electrons confined in electrostatically defined quantum dots hosted in silicon nanostructures. These act as "artificial atoms" (Fig. 2). Although the first quantum dot qubits were developed in GaAs/AlGaAs heterostructures, silicon has become favored due to three main advantages: higher operating temperatures, smaller footprint, and longer coherence times [22]. Beyond silicon, alternative materials such as indium arsenide (InAs) and hybrid superconductor-semiconductor platforms are also being explored for spin qubit implementations, offering potentially improved performance for some aspects. However, they often face scalability and industrial integration challenges, which silicon-based approaches mitigate [17]. A detailed discussion of these materials exceeds the scope of this review.

Two of the primary technologies used to realize quantum dot qubits are Si/SiGe heterostructures and SiMOS platforms, both of which achieve confinement using a combination of material interfaces and external electrostatic control. In SiMOS, charge carriers are confined in quantum dots formed in the silicon channel against a SiO_2 interface. The confinement is achieved through the electrostatic potential generated by lithographically patterned gates on top of the oxide layer [23]. In Si/SiGe, quantum dots are formed in a strained silicon channel between two SiGe layers on top and bottom, offering an ideal low-disorder environment [24], against the interface with the top SiGe layer. The confinement is similarly controlled via gate electrodes on top of the heterostructure (Fig. 2).

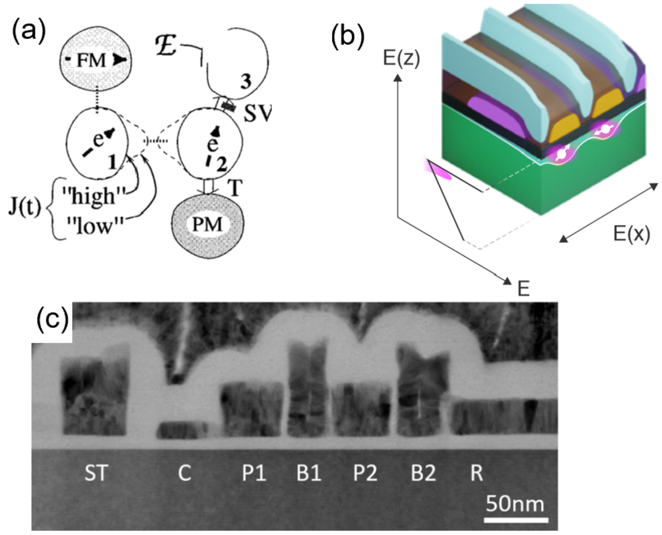

Fig. 2. (a) Schematic of Loss' and DiVincenzo's quantum-dot spin qubit proposal [18] (b) SiMOS device schematic including energy diagram showing electron confinement: confinement in the z-axis is provided by the Si/SiO_2 interface while in the xy-plane is achieved through the electrostatic potentials. Figure adapted from [17]. (c) SEM image of a SiMOS qubit device [25]

In addition to bulk CMOS processes, other industry-standard MOS technologies, such as Fully-Depleted Silicon-On-Insulator (FD-SOI) and FinFET, are also being explored for qubit applications. In FD-SOI, an extra insulating layer is introduced that separates the silicon channel from the substrate, minimizing leakage currents and increasing electrostatic control over the channel [26]. In FinFETs, the gate is wrapped around the silicon channel on three sides in a 3D structure vertically extended from the substrate, providing excellent electrostatic control and reducing short-channel effects [27]. Both FD-SOI and FinFET have demonstrated promising results for qubits [28], [29].

III. PERFORMANCE METRICS

The main requirements to build quantum computing hardware for achieving useful quantum computation are known as the DiVincenzo's criteria [32] and are the following:

1) A scalable physical system with well characterized qubits
2) The ability to initialize the state of the qubits to a simple fiducial state
3) Long relevant decoherence times, with respect to the gate operation time

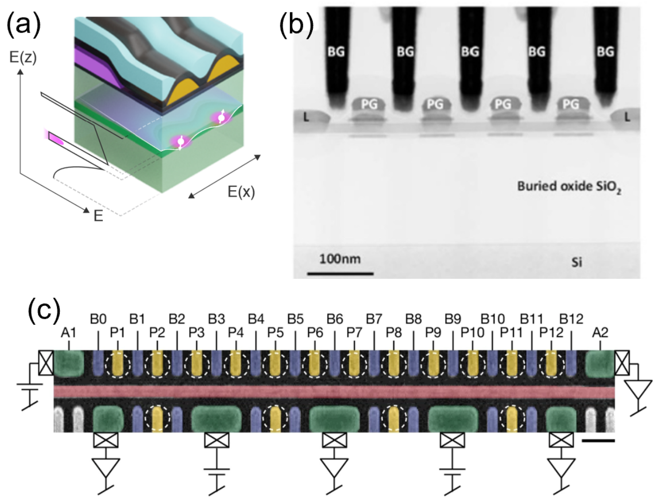

Fig. 3. (a) Si/SiGe device schematic including energy diagram showing electron confinement in the z-axis achieved by the Si/SiGe interface and in the xy-plane by the electrostatic gate potential. Figure adapted from [17] (b) TEM image of a linear quantum dot array in FD-SOI for qubit applications [30] (c) False-colored SEM image of a twelve-qubit processor in Si/SiGe [31]

4) A "universal" set of quantum gates
5) A qubit-specific measurement capability

Specific metrics have emerged in the literature in pursuit of meeting these criteria, of which we will define the most pertinent; the T_1 and T_2^* times, and one-qubit and two-qubit fidelities. The T_1 time is a measure of how long a qubit can remain in the $|1\rangle$ state before collapsing into the $|0\rangle$ state due to noisy interactions with the environment. The T_2^* time is a measure of dephasing of the qubit, giving an indication of unintended rotations around the z-axis of the Bloch sphere due to unwanted interaction with the environment. Long T_1 times have been achieved in silicon spin qubits, while T_2^* times are typically the bottleneck for these technologies, see Table. I for examples. The longer these times are, the more quantum operations can be carried out, allowing the realization of the third and fourth of the DiVincenzo's criteria. One and two-qubit fidelities are then a measure of the accuracy of one and two-qubit gate implementations in a given technology. Randomized benchmarking is a typical technique used here to measure the fidelity. This gives an indication of how many quantum gates can be applied before the accumulated error renders the qubits no longer useful. Therefore, as seen in Table. I, the goal is to ensure as high a fidelity as possible, with modern examples demonstrating fidelities exceeding 99% across one and two-qubit gates. The fidelities are not required to be increasingly accurate, there is a threshold beyond which quantum error correction techniques can be used to achieve the extremely low error rates needed for large-scale quantum computation [33]. One major trend to improve all of these metrics is the use of isotopically purified silicon, ^{28}Si, removing the ^{29}Si isotope with non-zero nuclear spin, which is a significant source of qubit decoherence in their environment [34].

Qubit Type	Donor	Si/SiGe	SiMOS [35]
T_1	$\sim$ 30s [36]	$>>$ 100μs [24]	$\sim$ 6s
T_2^*	$\sim$ 28μs/$\sim$ 1ms^a [37]	$\sim$ 4μs [24]	$\sim$ 30μs
1Q Fidelity	$\sim$ 99.9% [37]	$\sim$ 99.9% [24]	$\sim$ 99.9%
2Q Fidelity	$\sim$ 99.5% [37]	$>$ 99% [38]	$\sim$ 99%

TABLE I

COMPARISON BETWEEN VARIOUS SILICON-BASED QUBITS. ^{a} REFERS TO ELECTRON/NUCLEAR SPIN DEPHASING TIMES.

IV. QUANTUM-CLASSICAL INTERFACE

The classical electronics coupled to a quantum processor performs the following three functions: initialization, manipulation, and readout. The quantum-classical interface is designed to carry out all these operations with high fidelity, using several methods to process quantum information. For the sake of simplicity, we focus on one example integrating these three functions.

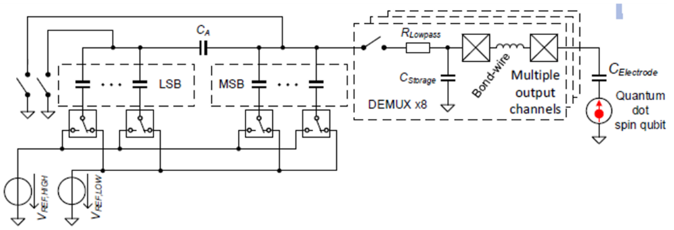

Fig. 4. Capacitive DACs utilized as voltage pulsers to initialize quantum dots. Figure adapted from [39].

The initialization process involves tunneling electrons from an electron reservoir into the quantum dot. This can be done by adjusting the dot confinement potential relative to the Fermi level of the reservoir. That potential is controlled by applying a voltage on the gate electrode directly above the quantum dot. In a more general case, the voltage at the gate needs to be dynamic in order to enable more complex functions useful when building interaction gates [35]. That functionality can be realized with capacitive DACs and one such implementation is shown in Fig. 4 from [39].

The next process is manipulation, in which the electron spin evolves corresponding to the desired quantum gate operation. This is achieved using Electron Spin Resonance (ESR), and is enabled by a time varying magnetic field from a current signal flowing through a nearby wire at microwave frequencies [40]. A simple gate operation, useful for this discussion, such as the Pauli X gate, evolves the spin of an electron in a quantum dot from the initial 'spin up' to 'spin down' state. The circuit architectures for this application are wide-band transmitters that contain several blocks such as VCOs, mixers, baseband DACs, PAs etc. and an example is shown in [41].

The last process is readout. The most practical method of measuring the spin of the electrons in a solid state device is indirectly through spin-to-charge conversion facilitated by a charge sensor [43], [44]. A more comprehensive discussion involves understanding the various spin state encoding schemes which is detailed in [45]. A charge sensor has a current flow that is highly sensitive to fluctuations in the local

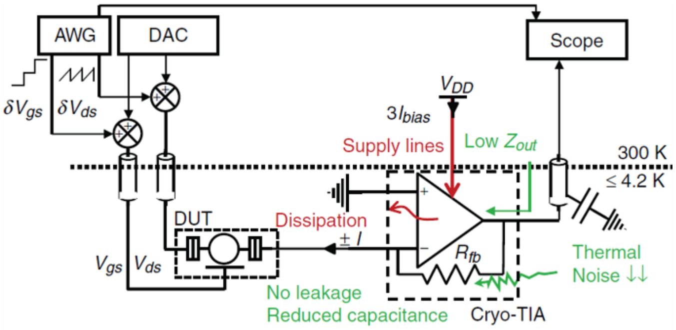

Fig. 5. Resistive transimpedance amplifier that measures the current from a charge sensor in order to determine the spin state. Figure adapted from [42].

electric field caused by the number of electrons in the nearby quantum dot. The small current through the charge sensor can be converted into a voltage through a high gain resistive transimpedance amplifier [42] (RTIA) as shown in Fig. 5. The input of the RTIA is directly coupled to the ohmic contacts connected with the charge sensor. The virtual ground of the RTIA sets the voltage bias across the charge sensor and the output voltage can be digitized with an ADC. Other readout techniques employ RF reflectometry where the charge sensor impedance is coupled to the occupancy state of the nearest neighbor quantum dot [43], [46].

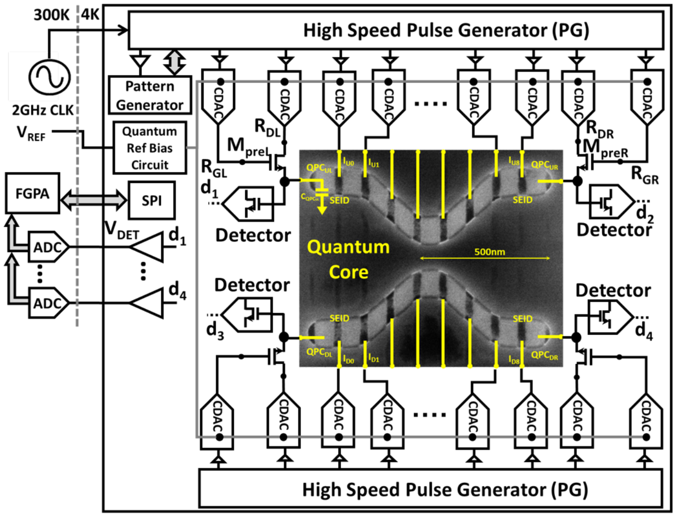

Fig. 6. Monolithic integration of Quantum Processor with cryogenic electronics. Figure adapted from [47].

Finally, we show an architecture employing monolithic integration of a quantum processor with the aforementioned cryogenic electronics in a single chip die fabricated in the 22 nm FD-SOI CMOS process from Global Foundries (Fig. 6 [47]). The integration of localized electronics removes the wiring bottleneck and achieves wide-band control and readout channels with extremely low parasitics. At the center of the block diagram is the quantum structure designed in an advanced lithography process. The gate electrodes are driven from high speed capacitive DACs that act as voltage pulsing circuits to control the evolution of the electron wavefunction in the quantum dot array. The four edges of the 'double-V' shaped structure connect with an interface device that allows control of electron flow from the reservoir to the nearest quantum dot. These nodes are also connected with the first stage of the detector, a source follower device. The detector outputs are discrete time and can be monitored from the test buffers that can be sampled by an off-chip ADC. The high speed pulse generator generates timing for the CDACs and the detectors according to a pattern defining the quantum experiment. That pattern is stored in cryogenic memory and is driven by the pattern generator block. That entire tile comprising the quantum structure and control electronics has an area of 250μm by 500μm and operates with a power budget of 2.5 mW per qubit [47].

V. COMMERCIALIZATION AND FUTURE CHALLENGES

Recent theoretical and experimental breakthroughs have demonstrated the potential of silicon technology platforms for quantum information processing, with applications in quantum computing, simulation, sensing, and more [20], attracting growing industry interest in spin qubits. Despite this progress, several technical challenges must be addressed before silicon spin qubits can achieve large-scale commercial realization. Key open questions and ongoing research efforts include improving qubit scalability and connectivity, enhancing fidelity, achieving operation at higher temperatures, mitigating charge noise, and optimizing cryogenic electronics for large-scale integration.

Leading modern computer industries, such as Intel and IBM, R&D centers, and start-ups are developing silicon-based donor and quantum-dot qubit architectures, along with their control and readout electronics. The list is not exhaustive and includes Imec (Belgium), Diraq and Silicon Quantum Computing (US, Australia), Quantum Motion (UK, Australia), TNO (Netherlands), CEA Leti and Quobly (France), Equal1 (Europe, N. America), ARQUE Systems (Germany), SemiQon (Finland), and HRL Laboratories (US) [48]. These worldwide efforts aim to leverage the decades of semiconductor expertise to advance silicon-based quantum computing.

VI. CONCLUSIONS

In this review, we outlined recent advancements in silicon-based spin qubits and their potential for scalable quantum computing. We presented various key architectures, including donor-based and quantum-dot spin qubits, assessing their key performance metrics. Furthermore, we discussed the classical control systems for qubit initialization, manipulation, and readout, highlighting the benefits of co-integration with cryogenic electronics to enhance qubit performance. While significant progress has been made, key open questions remain, such as improving high-fidelity operations and optimizing cryogenic electronics. With the growing interest of semiconductor industries, start-ups, and R&D centers, the future of this field appears promising and silicon spin qubits are expected to harness existing semiconductor infrastructures.

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