



located inside a cryo chamber, resulting in a long distance and heavy impedance load from the cryo chamber to the off-chip measurement components. In order to efficiently read the RO signal, 16 stages of  $\pm 2$  dividers are inserted before the output pad.

As previously shown in Fig. 2(a), different setup configurations for the proposed RO are feasible. Fig. 3(a) illustrates the simplest measurement configuration of the implemented system. In this sequence, the LDO is disabled and all four switches of the switch-cap sub-system are conducting, resulting in the direct connection between the supply line of the RO and the off-chip supply voltage source. In this setup, no supply noise reduction is obtained and so the supply noise is directly injected into the RO. Fig. 3(b) and (c) show the setup configuration that can help to reduce the injected noise from the supply voltage source into the RO. In this sequence, the LDO is enabled and it can provide power for the switch-caps. Fig. 3(b) illustrates the first half-period of the output RO clock when  $C_2$  is charging from the LDO while the  $C_1$  is providing supply for the RO. Fig. 3(c) shows the second half-period of the output RO clock when  $C_1$  is charging from the LDO while  $C_2$  is providing supply for the RO. The control signals for the charging/discharging of  $C_1$  and  $C_2$  are generated by the digital control unit inside the implemented system. The digital control unit uses the available clocking signal of the RO to provide the control signals. Fig. 3(d) illustrates the timing diagram of the working principle. When the LDO and switch caps are enabled, there will be a delay in starting the toggling of the switched-caps between the LDO and the RO supply line. This delay ensures that the caps have enough initially accumulated charge to feed the RO during the oscillation.

Fig. 3(e) shows the equivalent noise model of the supply voltage circuitry of the proposed RO. The model consists of the error-amplifier, output buffer of the LDO [4], switch capacitors, the RO and the voltage and current noise source models of the suggested system. Considering the equivalent output impedance of the LDO to be  $1/g_{m,M1}$ , the total output noise of the LDO can be estimated as [5]:

$$\overline{V_{n,LDO}^2}_{output} = \frac{\overline{I_{n|M2}^2}}{g_{m,M1}^2} + \overline{V_{n|Err-AMP}^2} + \overline{V_{n|M1}^2} \quad (1)$$

where,  $\overline{I_{n|M2}^2}$ ,  $\overline{V_{n|Err-AMP}^2}$  and  $\overline{V_{n|M1}^2}$  are the equivalent noise contributions from  $M_2$ , error-amplifier and  $M_1$ , respectively. The sw-cap components,  $C_{1,2}$  and  $M_{switch}$ , form a low-pass filter with the 3 dB cut-off frequency of  $f_0=1/2\pi C_{1,2}R_{M_{switch}}$ . The equivalent total LDO output noise is filtered by the sw-cap and the total supply voltage noise, which is injected to the RO supply line, can be calculated as:

$$\overline{V_{n,supply}^2} = \int_0^\infty \frac{\left[ \overline{V_{n,M_{switch}^2}} + \overline{V_{n,LDO}^2}_{output} \right]}{1 + \left( \frac{f}{f_0} \right)^2} df \quad (2)$$

$g_{m,M1}$  in the LDO is expected have a large value since the size of  $M_1$  and its current consumption are high. Also the the error-amplifier's MOSFETs inside the LDO have smaller sizes and lower power consumption, resulting in the domination of the

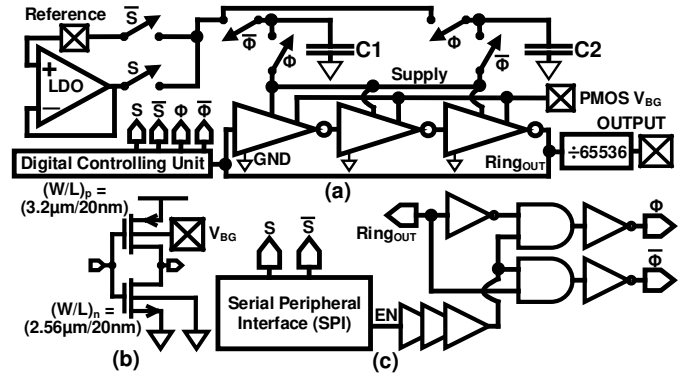


Fig. 2. (a) Top-level view of the proposed RO. (b) Delay cell. (c) Digital control unit.

error-amplifier noise in (1). On the other hand, at the CT, the thermal noise of the transistors decreases and the flicker noise becomes the dominating source of the noise [1]. Considering the corner frequency of the flicker noise (i.e.,  $f_c$ ) to be much smaller than  $f_0$ , the total supply voltage noise can be simplified as:

$$\overline{V_{n,supply}^2} \approx \int_0^{\frac{1}{2\pi R_{M_{switch}} C_{1,2}}} \frac{4kT\pi R_{M_{switch}}}{2} df + \int_{f_{min}}^{f_c} \frac{\alpha}{W_{Err-AMP} \times L_{Err-AMP} \times f \times (1)} df \quad (3)$$

where  $W_{err-amp}$  and  $L_{err-amp}$  represent the equivalent length and width of the MOSFETs in the error-amplifier,  $R_{M_{switch}}$  is the equivalent "on" resistivity of the  $M_{switch}$ ,  $T$  is the temperature and  $\alpha$  is the temperature- and mobility-dependent factor of the flicker noise in the error-amplifier. Equation (3) can be simplified as:

$$\overline{V_{n, Supply Voltage}^2} \approx \frac{kT}{C_{1,2}} + \frac{\alpha}{W_{Err-AMP} \cdot L_{Err-AMP}} \ln\left(\frac{f_c}{f_{min}}\right) \quad (4)$$

Equation (4) shows that the supply noise is dominated by the error-amplifier and appropriate MOSFET sizing is needed for it to minimize the injection of the supply noise to the RO. From [6], [7], the RO's PN due to the supply noise can be estimated as:

$$L(\Delta w) = \frac{\overline{V_{n, Supply Voltage}^2} \Gamma_0^2}{8\Delta w^2} \quad (5)$$

Equation (5) is calculated based on the assumption that high-frequency supply noise does not affect the PN of the RO [6]. From (4) it can be concluded that increasing the size of the MOSFETs in the error-amplifier and also increasing the size of  $C_{1,2}$  can reduce the PN (i.e., due to the supply noise) of the RO in the proposed system.

### III. EXPERIMENTAL RESULTS

The proposed techniques are implemented in 22-nm FD-SOI CMOS. Fig. 4(a) shows a zoomed-in portion of the chip micrograph that indicates the locations and layout of the fully integrated RO along with its controlling/sensing electronics. This includes the LDO, clock divider, digital control unit, RO and caps, which respectively occupy  $17.9 \times 38.7$ ,  $16.9 \times 12.8$ ,  $9.4 \times 3.8$  and  $136.5 \times 83.3 \mu m^2$ . The digital control system consumes 602 and 585  $\mu W$  at CT and RT, respectively; the core

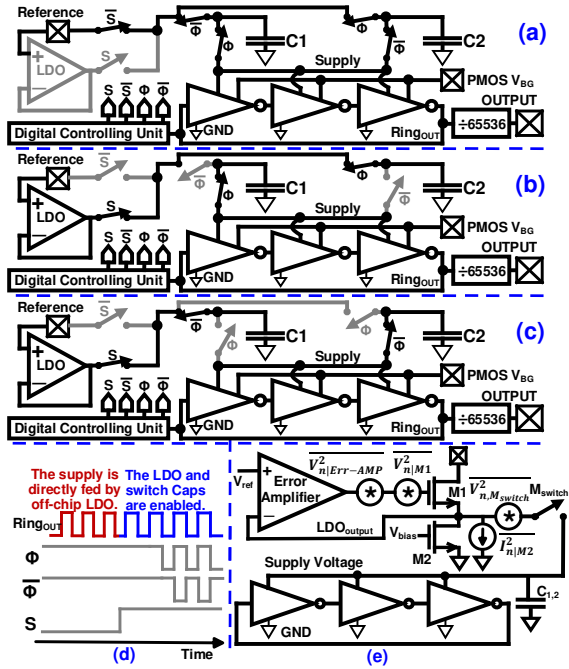


Fig. 3. Simplified architecture of the proposed RO when; (a) the supply is directly fed by off-chip LDO, (b) First phase of the switch-cap operation with LDO and phase reduction technique are enabled, (c) Second phase of the switch-cap operation with LDO and phase reduction technique are enabled. (d) Example waveform during the system operation. (e) Equivalent noise model of the proposed system.

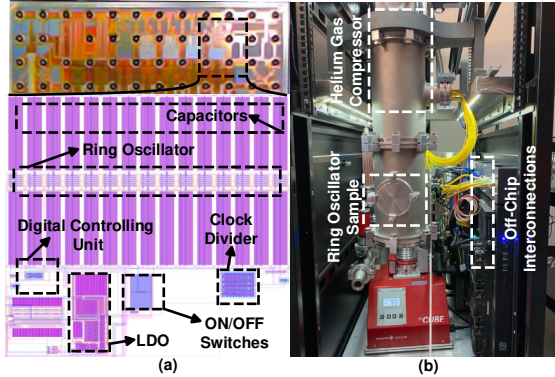


Fig. 4. (a) Die micrograph and the zoomed portion of the proposed RO. (b) Test setup for the proposed oscillator.

RO consumes 857 and 951  $\mu\text{W}$  at CT and RT, respectively; and the LDO consumes 107 and 67  $\mu\text{W}$  due to its quiescent current at CT and RT, respectively, when  $V_{BG}$  is 0 V. Fig. 4(b) shows a photo of the cryo chamber housing the quantum system. The fabricated chip is mounted on the printed circuit board (PCB) inside the cryo chamber, which is cooled down to  $<3.7\text{ K}$ .

Fig. 5 shows the effect of the LDO and switched capacitors on the RO PN, due to the rejection of the supply noise at RT. It can be observed that when the LDO and switch caps are enabled, the PN of the RO is reduced, indicating the effectiveness of the proposed method to reduce the supply noise and consequently reduce the PN of the RO. The integrated PN between 100 Hz to 10 kHz is measured as -60.89 dBc and -64.4 dBc when the PN reduction circuitry is disabled and enabled, respectively, at the RT. Fig. 6 illustrates

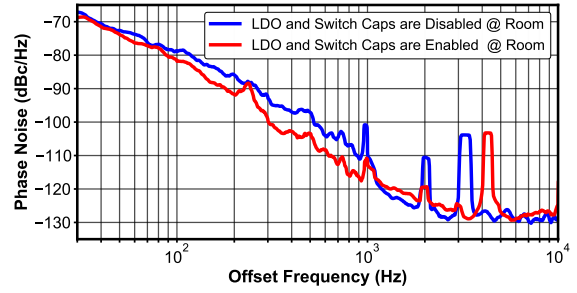


Fig. 5. Measured PN vs. offset frequency at RT when the LDO and the sw-caps are enabled and disabled.  $V_{BG}$  is 0 V.

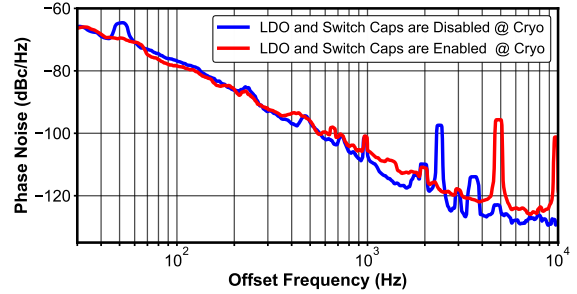


Fig. 6. Measured PN vs. offset frequency at CT when the LDO and the switch Caps are enabled and disabled and when the  $V_{BG}$  is 0 V.

the effect of the proposed PN reduction circuitry at 3.7 K. As it can be observed, still the enabled LDO and switch caps in the system can improve the PN of the RO, due to the reduction in the supply noise of the oscillator. The integrated PN between 100 Hz to 10 kHz is measured as -59.46 dBc and -59.7 dBc when the PN reduction circuitry is disabled and enabled respectively at the CT. At the CT, the resistivity of the metal tracks on the PCB and also inside the chip drops. As a result, the equivalent resistivity model of the tracks from the off-chip decoupling capacitors, into the chip and then into the supply line of the core of the RO will be reduced which then can provide better filtering and higher supply noise reduction in the oscillator. On the other hand, due to the drop in the metal resistivity at the CT, the on-chip decoupling capacitors, close to the core of the RO, will have better quality factors which results in lower supply noise in the system. As a result, at the CT, the supply noise is already reduced due to better filtering, which can explain the less improvement of the PN when the LDO and switch caps are enabled in the system, comparing the CT with RT results in Fig. 6 and Fig. 5 respectively.

Fig. 7 plots the measured PN when the LDO and sw-caps are enabled for both CT and RT. The integrated PN between 100 Hz to 10 kHz is measured at -59.7 dBc and -64.4 dBc at CT and RT, respectively. By enabling the LDO and the sw-caps, the effect of the voltage supply noise on the PN can be reduced, and as a result the dominant source of PN can be the internal transistor noises. With this setup, it is possible to measure the effect of temperature on the corner frequency of the flicker noise (i.e.,  $f_c$ ). The external power supply setup is at the RT and has the same configuration for both the RT and the CT measurements. Also, the voltage supply noise is further reduced by enabling the LDO and the sw-caps,

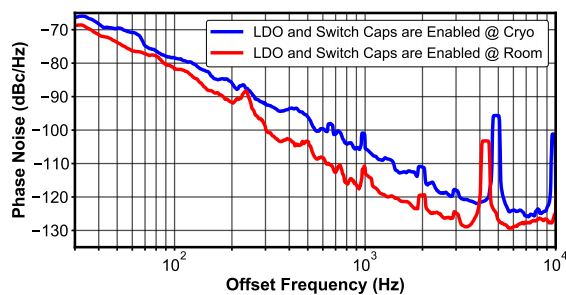


Fig. 7. Measured PN vs. offset frequency when the LDO and the switch Caps are enabled, at RT and CT and when the  $V_{BG}$  is 0 V.

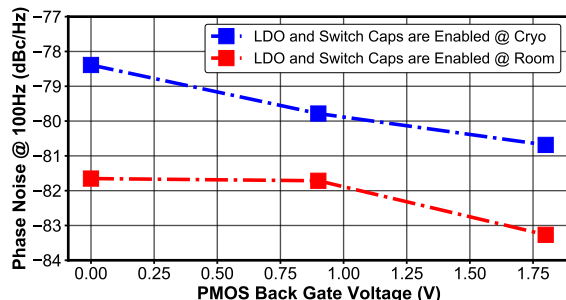


Fig. 8. Measured PN vs. PMOS back gate voltage when the LDO and the switch Caps are enabled, at RT and CT.

resulting in the dominance of the MOSFET's flicker noise on the output PN of the RO. The slope of the PN in Fig. 7 is 30 dB/decade, which is within the frequency window of the up-conversion of the flicker noise to the PN in the RO. Fig. 7 shows the increase of  $f_c$  at the CT compared with the RT, (also reported in [1]), by indirectly measuring the PN of the RO within the 30 dB/decade frequency window. Flicker noise at CT needs further investigation; elaboration of the physical reasons behind the change of the flicker noise from RT to CT is beyond the scope of the paper.

Fig. 8 illustrates the measured PN at 100 Hz frequency offset for three different PMOS back-gate voltages of the RO, at RT and CT. In general, Fig. 8 shows higher PN for the RO, compared with the measurement results at the CT, with the RT as also was discussed in Fig. 7. In the 22-nm FD-SOI technology, increasing the PMOS back-gate voltage (i.e.,  $V_{BG}$ ), increases  $V_t$  of the PMOS transistor inside the oscillator, which slows down the oscillating frequency of the RO. The measured down-divided oscillating frequency changes from 14.6 to 10.7 kHz at the CT and from 15.7 to 11.48 kHz at the RT, when the LDO and sw-cap system are enabled and when  $V_{BG}$  changes from 0 to 1.8 V, respectively. Based on [6], the asymmetry of the rising and falling edges of the ring oscillator's outputs results in the increase of the impulse sensitivity function (ISF) of the RO, which eventually leads to the increase of the PN. In 22-nm FD-SOI technology, back-gate voltage can be used as the MOSFET's charging/discharging slope tuning tools to balance the two falling and rising edges of the RO signal to improve the PN of the oscillator.

Performance summary and comparison with prior art are presented in Table I. The PN and FOM are estimated from

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART.

Reference	[8]	[10]	[11]	[9]	This Work
Process (nm)	65	28	65	65	22
Power @CT [mW]	N/A	N/A	N/A	N/A	0.857
Power @RT [mW]	0.65	1.16	1.1	1	0.951
Inherent Freq. Div. Output	5	No	No	No	65536
Osc. Freq @CT (MHz)	N/A	N/A	N/A	N/A	957
Osc. Freq @RT (MHz)	1700	3000	1600	1000	983
PN @CT [dBc/Hz]	N/A	N/A	N/A	N/A	-117.7
PN @RT [dBc/Hz]	-49.7	-26	-22.9	-38	-122
FOM @CT [dBc/Hz]	N/A	N/A	N/A	N/A	121.7
FOM @RT [dBc/Hz]	156	134.9	126.6	138	124

10 kHz offset oscillating frequency. The proposed oscillator is the first report of a RO at CT.

#### IV. CONCLUSION

This paper demonstrated an inverter-based RO, suitable for quantum computing applications. The proposed system occupies less than 0.012 mm<sup>2</sup> and can reduce the integrated PN of the RO at RT more than 3.5 dBc by means of the proposed voltage supply noise isolator system. The flicker noise was observed to increase from RT to CT by indirectly measuring the PN of the RO, showing the increase of 4.3 dBc/Hz PN at 10 kHz. The effect of  $V_{BG}$  on the PN of the RO was illustrated. It was also shown that by driving the noise model of the system that the flicker-noise of the error-amplifier inside the LDO is the dominant source of the supply noise of the RO in the proposed system.

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