Performance of Ring Oscillators for Cryogenic Electronics Integration from 4 to 200 K

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***Abstract*—In this paper, we present the characterisation of ring oscillator (RO) test circuits fabricated in GlobalFoundries' (GF) 22 nm fully depleted silicon-on-insulator (FD-SOI) process and operating from 200 K down to 4 K. We investigate ROs using NAND, NOR, and inverter standard cell libraries, including low, regular, and high threshold-voltage versions. Alongside temperature variations, we also consider a change in the power supply of $\pm 5\%$ from a nominal 0.8 V. The ROs demonstrate the combined effect of increased mobility, increased threshold voltage, and leakage current processes at cryogenic temperatures on their operation. By averaging over 81 fabricated ROs using three different delay gates and 2 different flavours, we report a statistical characterisation of their properties in the FD-SOI technology over temperature and supply voltage.**

***Index Terms*—ring oscillator (RO), CMOS, silicon-on-insulator (SOI), cryogenic, leakage**

I. Introduction

The study of CMOS integrated circuits (ICs) at cryogenic temperatures is motivated by its numerous applications, ranging from high-energy physics [1] and radio astronomy [2] to quantum computing [3] and many more. In the space of quantum computing, the co-integration of CMOS ICs on the same substrate as the qubit structures promises scalable architectures needed for practical quantum computation [3].

Compact modelling [4]–[6] and characterisation of integrated devices at cryogenic temperatures [7]–[11] is a highly active area given the current lack of industry standard cryogenic models. A number of features arise in such cryogenic characterisations of transistors, including increased threshold voltages, subthreshold slopes, and electron mobility.

Designing ICs in the presence of these cryogenic effects necessitates changes in the design methodology that is normally employed at room temperature (RT). As a test vehicle for cryogenic ICs, we investigated one of the most popular circuits for such work, ring oscillators (ROs), incorporating many repeating standard cells, and thus a test of repeatability of integrated design at cryogenic temperatures [12]. The choice of ROs as a testbed is further motivated by their many applications at cryogenic temperatures including temperature sensing [13]–[15], total ionization dose (TID) structures [16], foundation of phase-locked loops (PLL) [17], and even as a method to estimate noise signatures, including charge and flicker components, over temperature [18].

We report an extensive characterisation of three implementations of RO architecture across temperature and supply voltage in GF's 22 nm FD-SOI process. A unique feature of SOI processes includes the back gate, which can be used to dynamically vary the threshold voltage, and thus power consumption [10]. The ROs are shown to still function at cryogenic temperatures at a nominal supply voltage, with a clear variation of the oscillation frequency over temperature and a correlation with leakage current and threshold voltage temperature dependencies. The variation in the oscillation frequency over temperature provides an insight into semiconductor conduction processes and their dependence on temperature.

II. Experimental Methodology

The basic methodology behind this study is summarised as:

- Build a characterisation structure with repeating cells.
- Each cell contains the same RO circuit architectures using inverter, NAND, and NOR standard cells. The standard cells are mostly the regular-threshold and low-threshold devices.
- The variation in output frequency over temperature and supply voltage is then monitored for all ROs in each cell while warming them up from 4 K to approximately 200 K.
- The process is then repeated for a range of supply voltages, with the same sweep in temperature.
- Given the number of cells in the characterisation structure outlined in the following section, statistics can be constructed on the operation of ROs in this technology over temperature.
- A number of design regions are then identified based on the statistical characterisation, aiding in the future design and use of ROs in FD-SOI technology.

III. Characterisation Setup

In carrying out the methodology outlined in Section II, we designed a test chip with repeating unit cells, as shown in Fig. 1. The chip is placed inside a cryo-cooler operating at ~ 4 K, see [19] for further details. Fig. 1a shows the test chip mounted on its PCB. The chip micrograph is shown in

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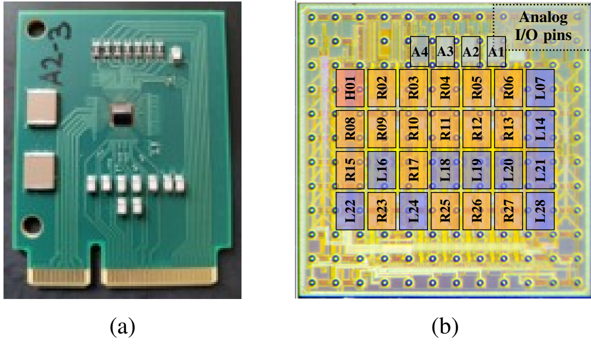

Fig. 1: (a) The testchip mounted on a PCB. (b) Chip micrograph: cells in the center (labeled 1 to 28) contain ROs, and a grid of further devices is shown on the top, labelled A1–A4.

Fig. 1b, highlighting the repeating unit cells. There are three types of ROs contained in each cell, labelled 1–28 in Fig. 1b. The letters 'H', 'L', and 'R' stand for high, low, and regular threshold-voltage ($V_{\rm th}$) standard cells, respectively. Further test devices, labelled A1–A4, were discussed previously in [19].

A simplified schematic of the ROs in the repeating cells is shown in Fig. 2. Each cell contains three ROs, one made of inverters, one of 4-input NOR gates, and one of 4-input NAND gates. The inverter is the fastest available in the library at the nominal operating conditions, with the NAND and NOR gates chosen as their slowest versions. Each oscillator consists of 60 logic gates plus a NAND gate to enable/disable its output. The measured output frequency is labelled f_0 in Fig. 2. All measurements were performed at zero back gate voltage. A simulation of the distribution of threshold voltages for the core devices at room temperature is shown Fig. 3. Note the LVT device has a higher threshold voltage than the RVT device.

Maintaining the density of measurement points over temperature was difficult given the rapid rise from 4 K once the fridge was deactivated. Therefore, the measured data is less dense at lower temperatures, which can be seen in the presented measurements in Section IV, followed by a discussion of the results in Section V.

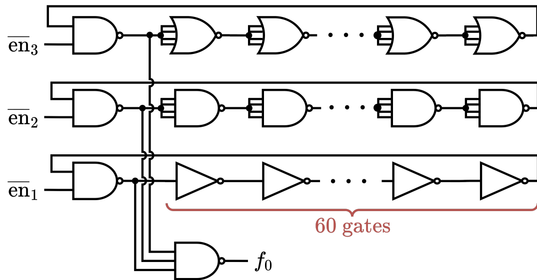

Fig. 2: Schematic of the NOR, NAND, and inverter-based ROs included in each cell. There are total of 60 gates of each NOR, NAND, and inverter types, followed by 2-input NAND gates to enable/disable the outputs. All oscillator outputs are fed into the final 3-input NAND used to merge the outputs into one. The output frequency is labelled as f_0.

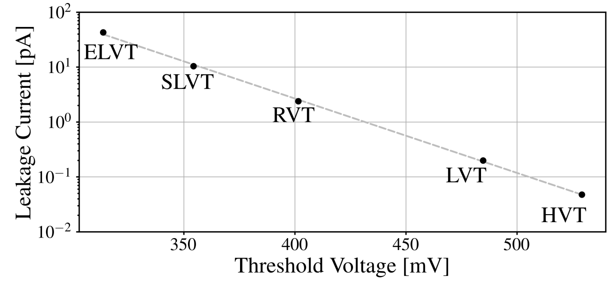

Fig. 3: Simulated leakage current versus threshold voltage of core (0.8V) devices in GF's FD-SOI process at RT in the typical corner. The back gate voltage is 0 V.

IV. Ring Oscillator Measurement Results

All ROs were measured for different temperatures and supply voltage conditions. The results for the high-$V_{\rm th}$ ROs in cell 1 in Fig. 1b are not included in this analysis as there is only a single high-threshold cell.

The output frequency of the regular-$V_{\rm th}$ ROs over temperature is shown in Fig. 4. This is at a nominal supply voltage of 0.8 V. As mentioned previously, due to the rapid increase of temperature from 4 K, there is a lower density of measurements at lower temperatures. The cell to cell variation over the regular-$V_{\rm th}$ ROs is approximately 2 %.

A linear fit of the measured frequency in the left and right of Fig. 4 provides rough indications of the boundaries between the regions labelled I, II, and III. These regions

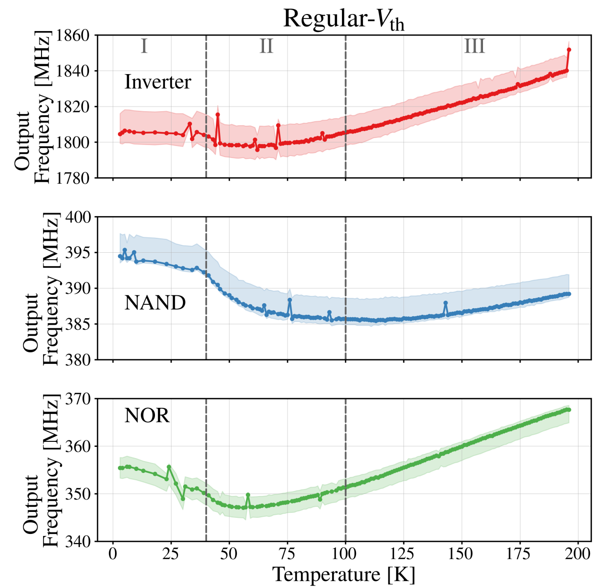

Fig. 4: Measured output frequency of regular-$V_{\rm th}$ ROs with a nominal supply of 0.8 V. The central line shows the median over the repeating regular-$V_{\rm th}$ cells. The shading shows the interquartile range. Three regions (I, II, III) highlight the variation in the frequency response over temperature from linear to non-linear to linear again.

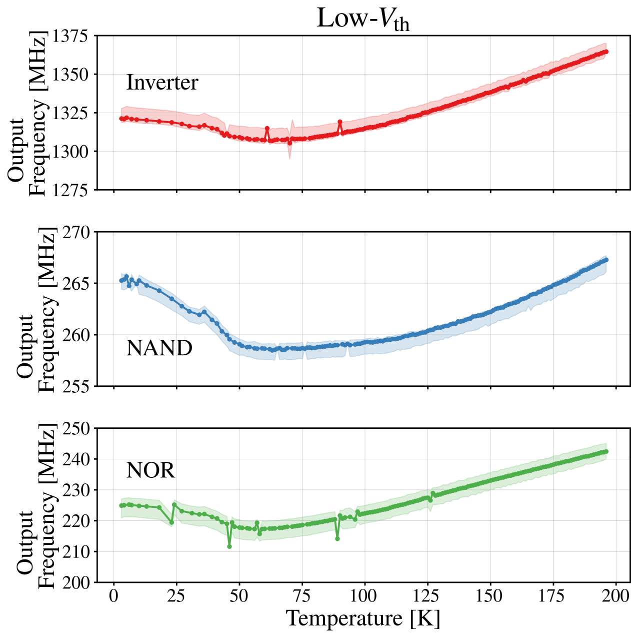

Fig. 5: Measured output frequency of low-V_{th} ROs with a nominal supply of 0.8 V. The central line shows the median over the repeating low-V_{th} cells. The shading shows the interquartile range.

denote the change in the frequency-temperature response of the RO design regimes. Region I (4 K $\rightarrow$ 30 K) shows an approximately linear response of the output frequency at deep cryogenic temperatures. Region II (30 K $\rightarrow$ 100 K) shows a non-linear response in the output frequency. Finally, region III (100 K $\rightarrow$ 200 K) shows again a linear response of the output frequency. Further discussion of the physical processes underlying these regions and their implications on design is presented in Section V.

The same measurements were taken for the low-V_{th} ROs, see Fig. 5, with very similar trends over temperature as in the regular-V_{th} ROs. The oscillation frequency range is lower, as we would expect given the behaviour of the threshold voltage in Fig. 3. Assuming that the oscillator frequency is strongly dependent on the current from the RO delay stage while the load capacitance between the various core device flavors is the same, then we expect a higher output frequency for devices with lower threshold voltage and vice versa. Similar design regions can be identified visually as done in Fig. 4. There are some gaps in the interquartile range calculations due to the availability of measurement data from all low-V_{th} cells at all recorded temperatures; however, the general trend is still visible.

The variation in the output frequency over temperature for various supply voltages was then measured for both the regular-V_{th} and the low-V_{th} ROs, see Fig. 6 and Fig. 7, respectively. Outside of the reported supply voltage range (0.75 V $\rightarrow$ 0.85 V), the oscillators would typically fail upon reaching both high temperatures and cryogenic temperatures

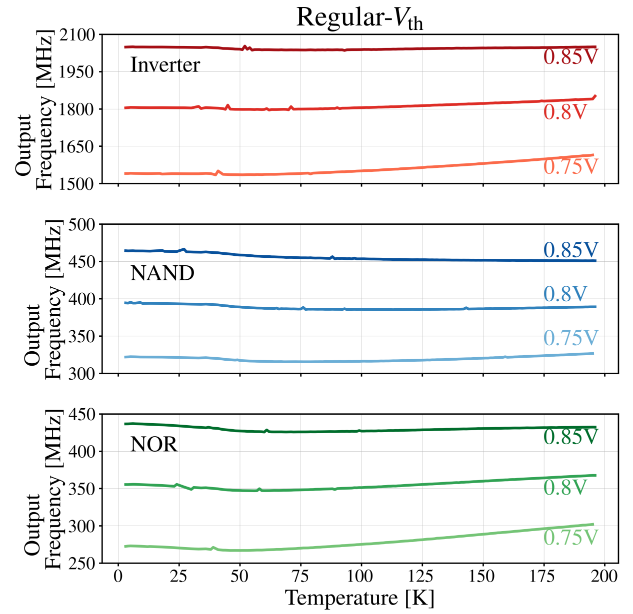

Fig. 6: Measured median output frequency vs. temperature of regular-V_{th} ROs with a varying supply voltage from 0.75 V to 0.85 V.

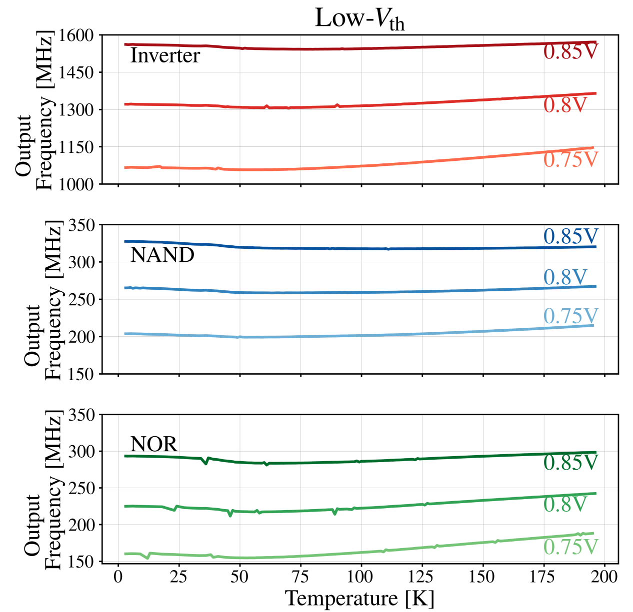

Fig. 7: Measured median output frequency of low-V_{th} ROs with a varying supply voltage from 0.75 V up to 0.85 V.

and so these results are not included in this work.

We note that a similar variation in the output frequency is seen with the varying supply voltage over temperature as we saw in the nominal supply case. Therefore, it is also possible to split these measurements into the same three regions as done in Fig. 4. Given the ubiquitous nature of the measured RO frequency response over temperature and supply voltage, we argue in Section V that the explanation lies in

semiconductor conductivity mechanisms and their dependence on temperature.

V. Observations and Design Recommendations

We now look at some of the underlying semiconductor conductivity mechanisms that contribute to the shape of the frequency-temperature responses in Section IV. This is an initial qualitative discussion and more extensive analysis will be carried out in future work.

Region III in Fig. 4 extends down to approximately 100 K, aligning with the end of the extrinsic temperature region where the carrier concentration is dominated by the dopant concentration [20]. Therefore, the region III to region II transition appears to be partly explained by the extrinsic to freeze-out transition in the majority-carrier concentration.

Following the same logic, region II in Fig. 4 would then be partly explained by the partial ionisation of the majority dopant concentration. Although a device-type and bias dependent effect, it is also noted in [10] that there is an increase in the on-state current, more so for long-channel nMOS devices but also for short-channel nMOS devices below 100 K, whilst there is a decrease for pMOS devices. We also note the greatly increased electron mobility below approximately 77 K in [9], [10]. Both of these factors may contribute to the increased switching speeds as we transition from region II to region I, thus correlating with the increase in the RO output frequency.

The increase in mobility at deep cryogenic temperatures is typically attributed to the variation in the dominant scattering processes over temperature. There are four major scattering processes noted in [6] that determine the mobility: phonon scattering, Coulomb scattering, surface roughness, and inter sub-band scattering. Generally, the phonon scattering process is greatly reduced at lower temperatures, given the reduction in thermal noise, so there is an effective increase in the mobility. However, the scattering due to surface roughness becomes more dominant at these lower temperatures, resulting in a saturation of the mobility [5].

We can also correlate our measurement results with those found in [21] for the very same technology, which are reproduced here in Fig. 8. Note the frequency-temperature response measurements are taken up to approximately 200 K. The gate leakage current in general will be a function of the underlying semiconductor conduction processes noted earlier, so these measurements allow an approximate insight into the physical processes at work over temperature [22]. Observe the decrease in the gate leakage current in Fig. 8 as we move from $\sim$200 K down to $\sim$125 K, roughly correlating with region III. We then see the leakage current remains close to zero from $\sim$125 K to $\sim$75 K, somewhat offset from the region II response. Finally, we see an increase again in the leakage current below $\sim$75 K, approximately corresponding to the region I frequency-temperature response. The device sizing differs somewhat in [21] to that investigated here, however there is a clear correlation between the gate leakage current over temperature and the RO frequency response over temperature noted in this work.

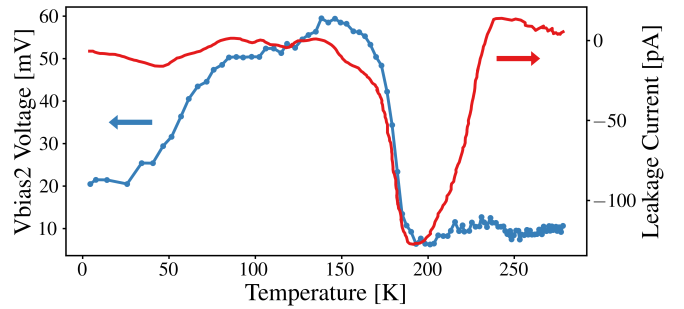

Fig. 8: Data reproduced from [21]. The trigger level of Vbias2 over temperature for a fixed CDAC code for 160 μsec delay pulse is shown in blue. The calculated leakage current is plotted in red over temperature on the same plot. The voltage Vbias2 allows us to probe the variation in the CDAC switching threshold, giving an insight into the gate leakage current dependence over temperature. The voltage over temperature is a measured quantity and the leakage current is derived from these measurements. See [21] for further details.

We make some final comments on the three regions identified in Fig. 4. We refer to these as three distinct design regions, depending on the temperature of the application. Firstly, we highlight that the studied ROs operated over a wide range of temperature, including a deep cryogenic range of a few Kelvins, making these fundamental circuits usable in quantum control circuitry or other applications requiring colder temperatures. We also note that due to a distinct, non-linear variation in the output frequency as a function of temperature, application specific design techniques should be applied depending on the regions we identify in this study. For example, the linear design regions, I and III, admit a straightforward characterisation of the ring oscillators. However, designing and biasing an RO for use at temperatures in region II, in the range of liquid nitrogen ($\sim$77K), may prove more difficult due to the nonlinear frequency-temperature response. We note that these temperature dependent variations appear to be a persistent property and are manifested for different designs of the RO delay cell.

VI. Conclusions

This work presented a statistical analysis of ROs using inverter, NAND, and NOR regular- and low-V_{th} standard cells in GF's commercial 22 nm process. A number of regions were noted in the frequency-temperature response of the ROs over temperature, which can be largely explained by the variation in semiconductor conduction processes over temperature. We also noted the correlation with the gate leakage current measured in [21] using the same fabrication technology. Similar design regions can also be seen with a $\pm 5\%$ supply voltage variation on the ROs. This work should aid in the future design and use of ROs from deep cryogenic temperatures, up to liquid nitrogen temperatures, and above.

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