Characterization of Silicon based Spin qubits in a 22nm Commercial FD-SOI Process

Session S74.00012

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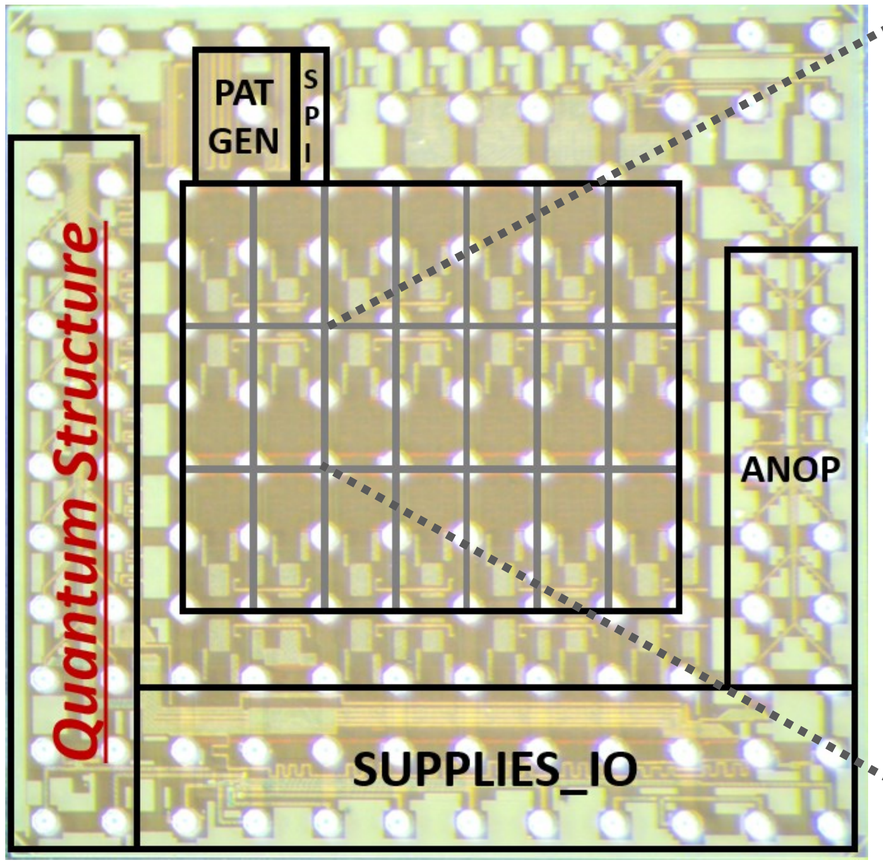
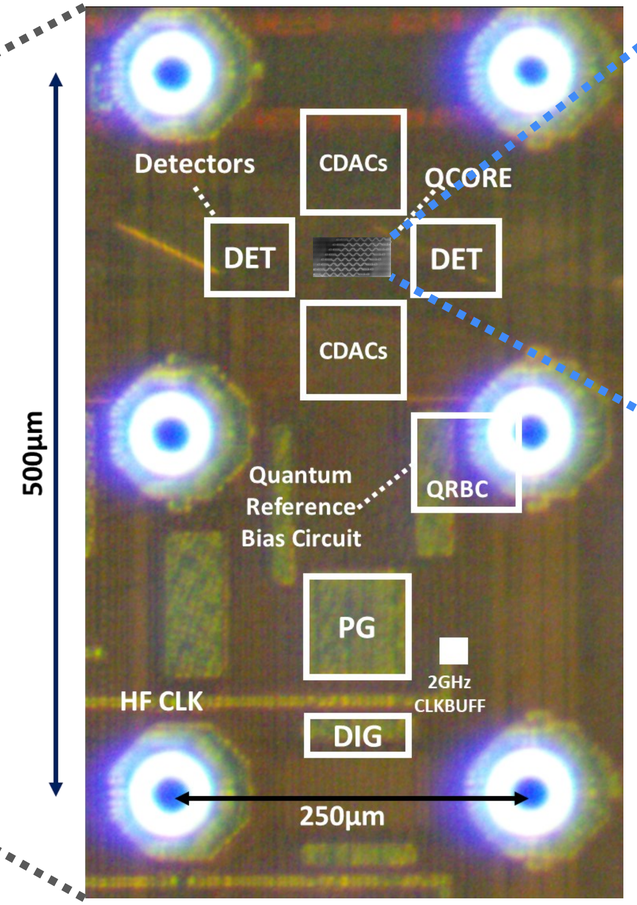
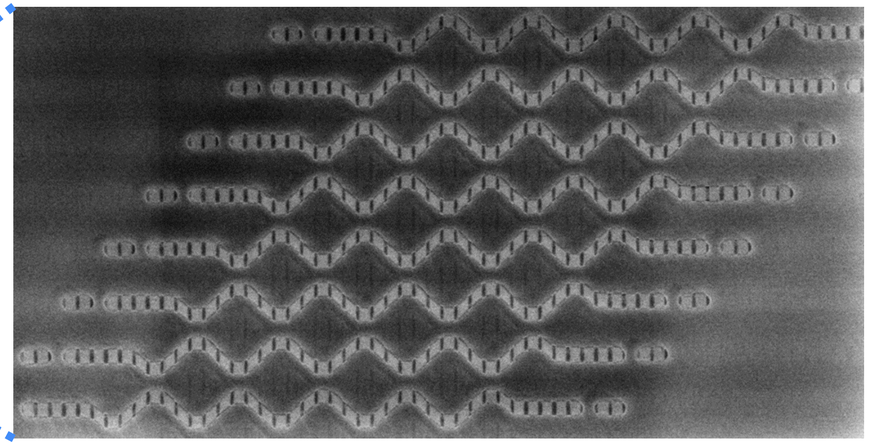
Equal1 Quantum Computer

- Desktop size quantum computer comprising compressor, cryocooler, vacuum pump, motherboard & airside PCB
- DC bias on flex lines & RF Signals on coax
- < 2-ft (internal) cabling
- 200mW cooling power
- 3.3K Base Temperature
- 1.5kW power consumption (110V / 16A Single Phase)

Integrated Quantum SoC





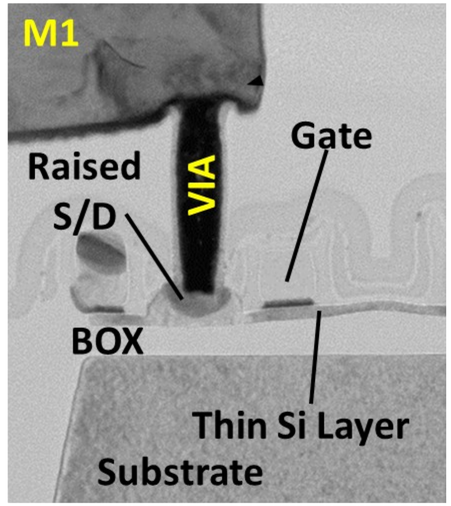


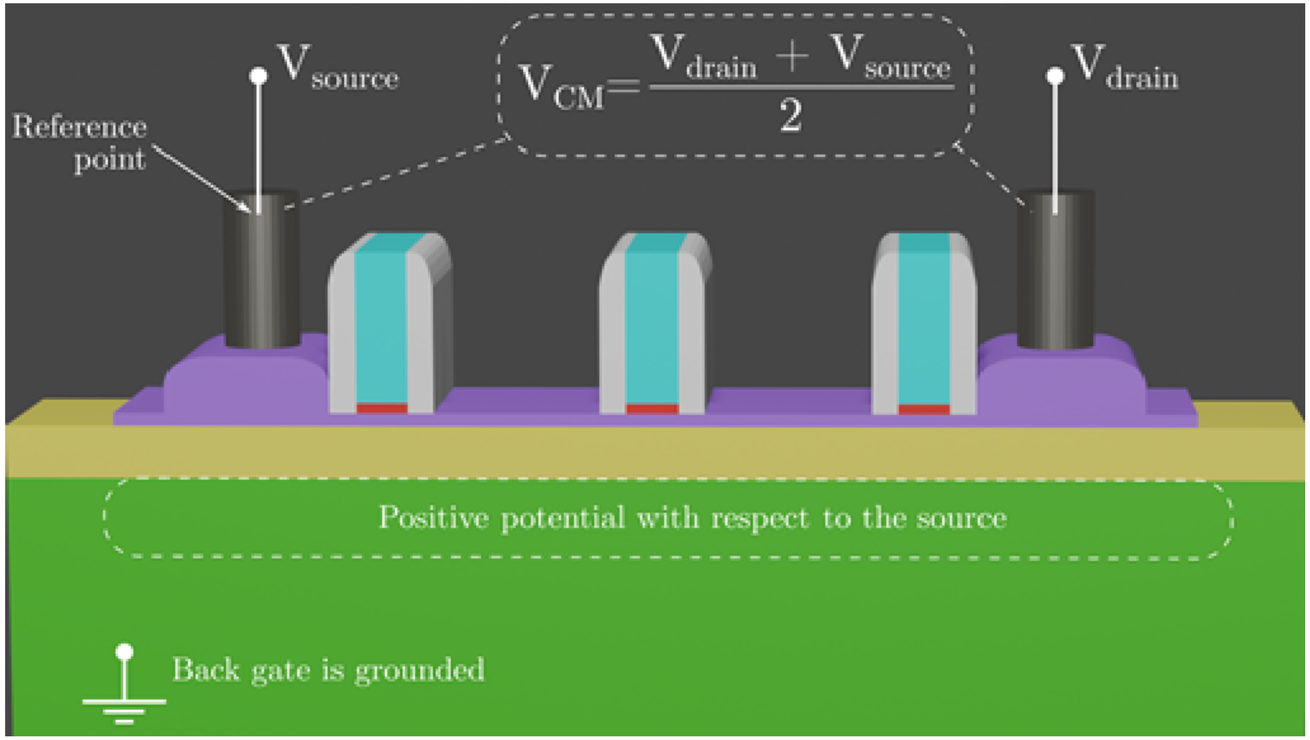
- 240 Quantum Dots
- 8 Detectors
- 32 Capacitive DACs
- 3 DC Bias Generators
- 2.5mW / qubit thermal load due to integrated control & readout electronics

"Monolithic Integration of Quantum Resonant Tunneling Gate on a 22nm FD-SOI CMOS Process"; arXiv:2112.04586

Quantum structure

- Fabricated in 22nm CMOS FDSOI Process from GlobalFoundries
- Lateral confinement dimensions ~70 x 70 nm^2, separation ~ 20 nm barrier
- Effective confinement in thin intrinsic Si layer (4nm)
- Channel electric field control by gates and common mode voltage





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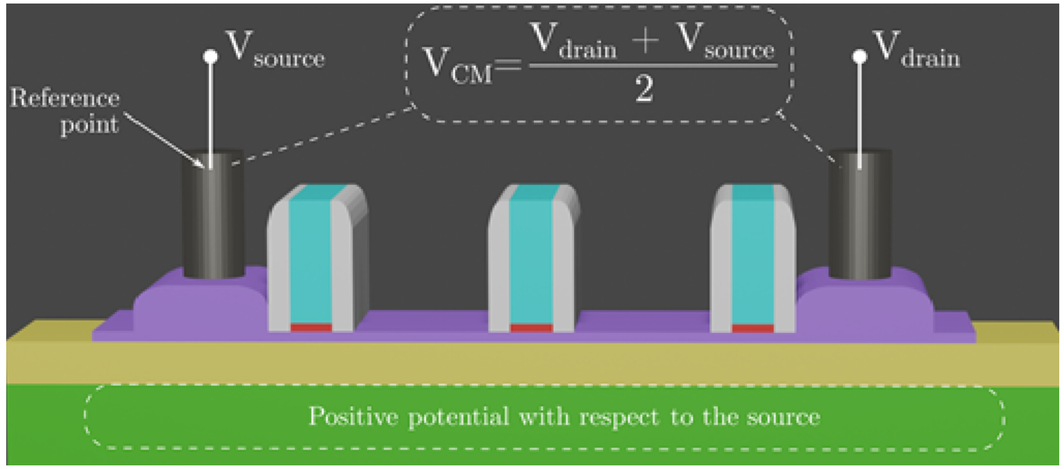
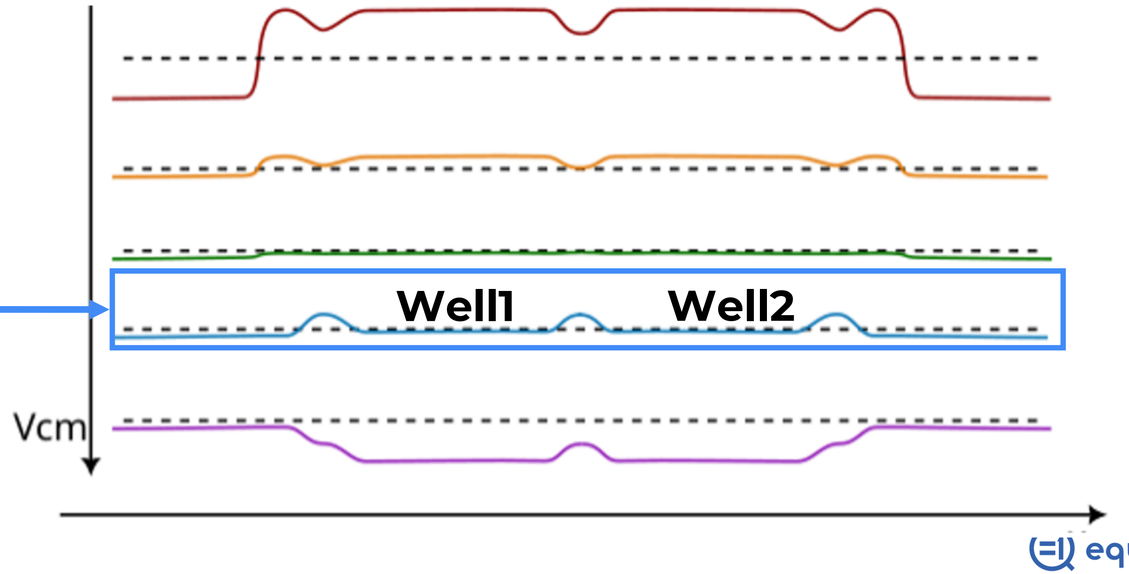
Common mode control

- Back gate is ground.
- Common mode voltage makes the potential on the source and drain negative with respect to ground.
- As a result, the common mode works as a single global plunger.

Dual Quantum Dot Mode
with small tunneling barrier





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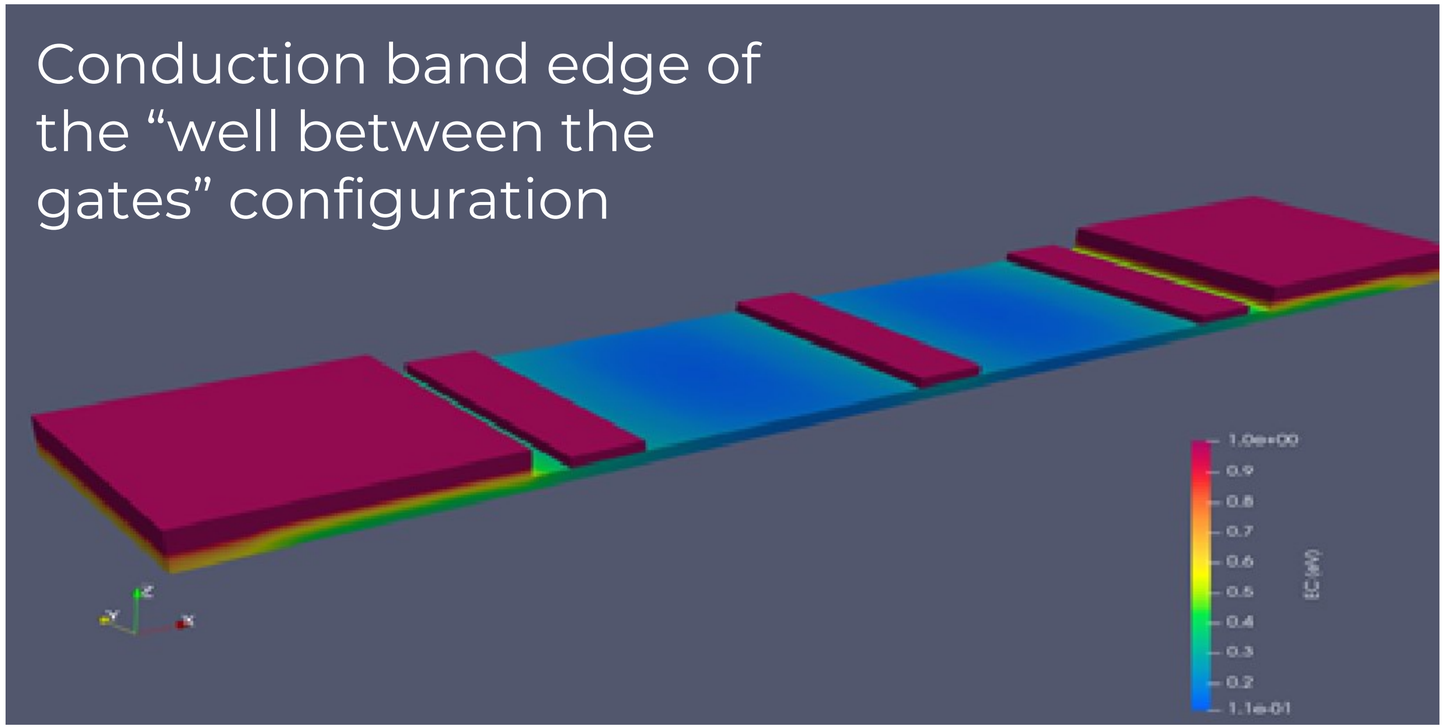
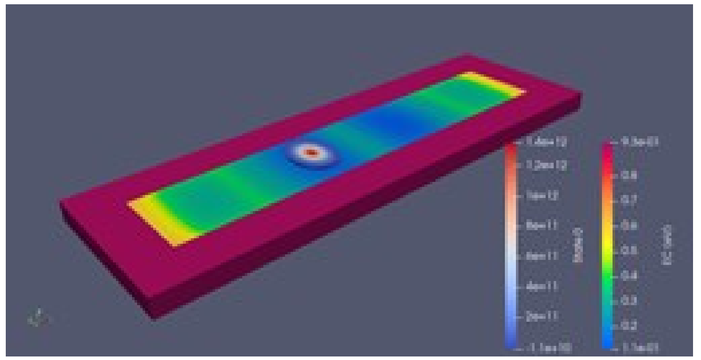
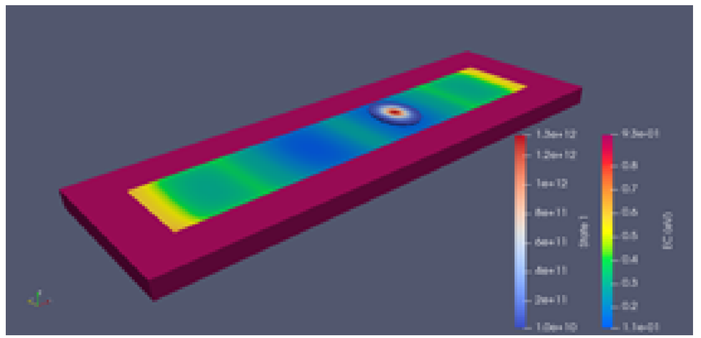
QTCAD Simulations

- Solve the Poisson or Poisson Schrodinger equations at cryogenic temperatures.
- Calculate the conduction band edge, single-electron wavefunctions & quantum transport properties of the device (coulomb peaks).



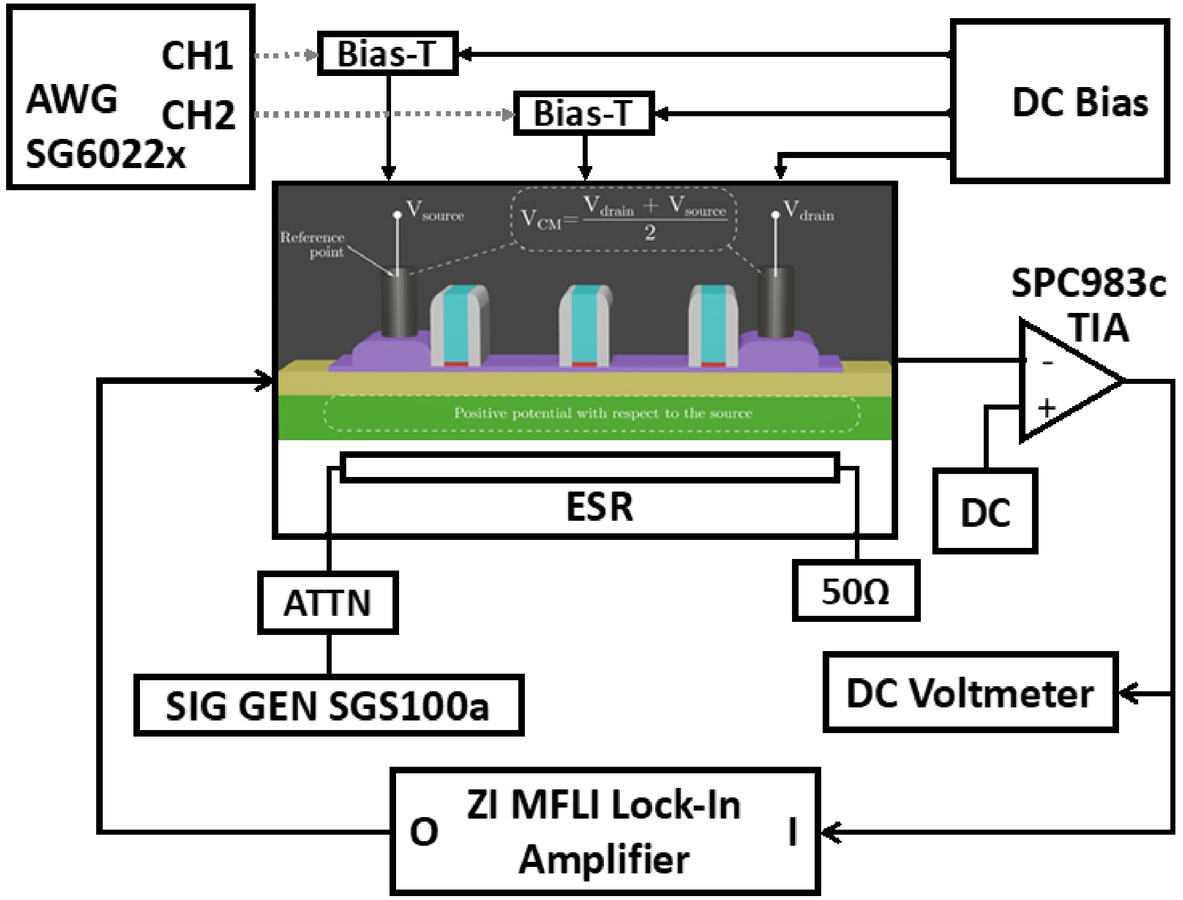




Measurement Apparatus

- Low noise DC supplies control barrier gates
- ARBs allow pulsing of barrier gates to bias structure into Coulomb Blockade regime
- Drain is excited by ZI MFLI Lock-In Amplifier
- Transport current converted to voltage by Basel Instruments SPC983c TIA
- Current noise floor limited by TIA

- $\sigma_i = \sqrt{i_{PSD}^2 \bullet \Delta f} = 6.3 f A_{rms}$ in 1.6Hz measurement bandwidth or 100ms TC.



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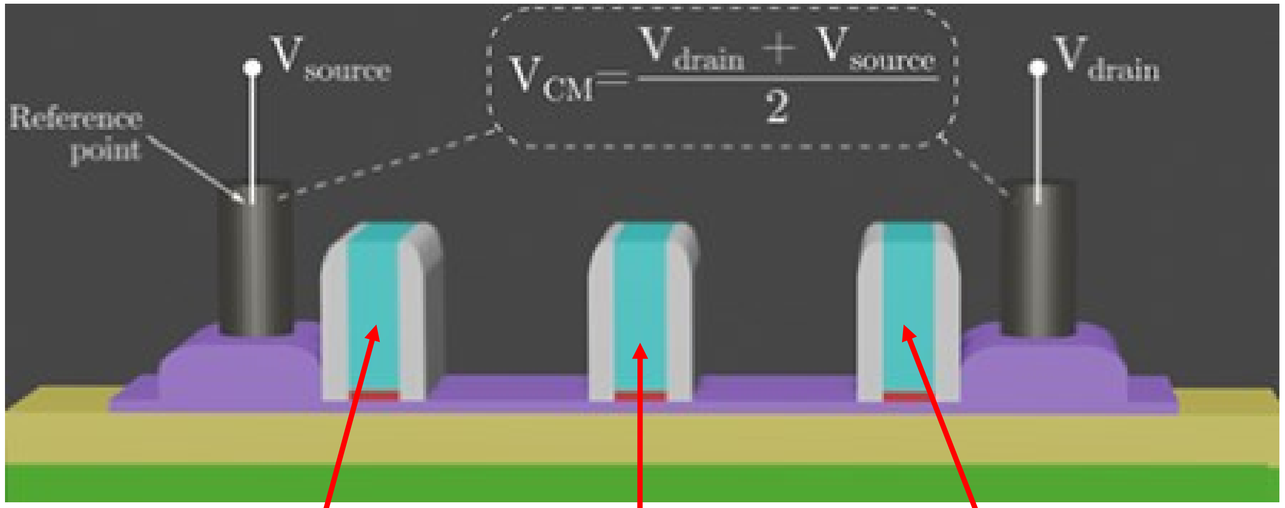
Measurement: conduction conditions

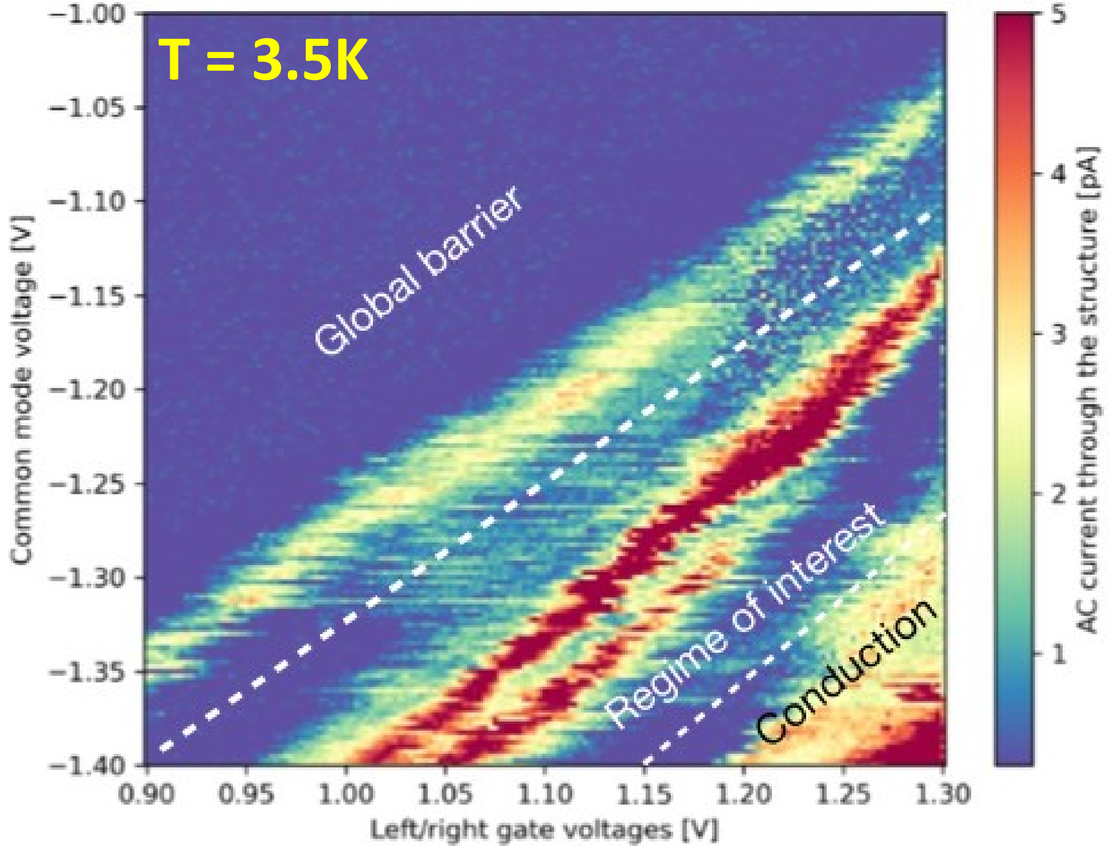


Left Gate Voltage

Middle Gate Voltage

Right Gate Voltage

Sweep Left/Right gate voltages & Vcm & measure the drain-source conductance.



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Measurement: charge stability (1)

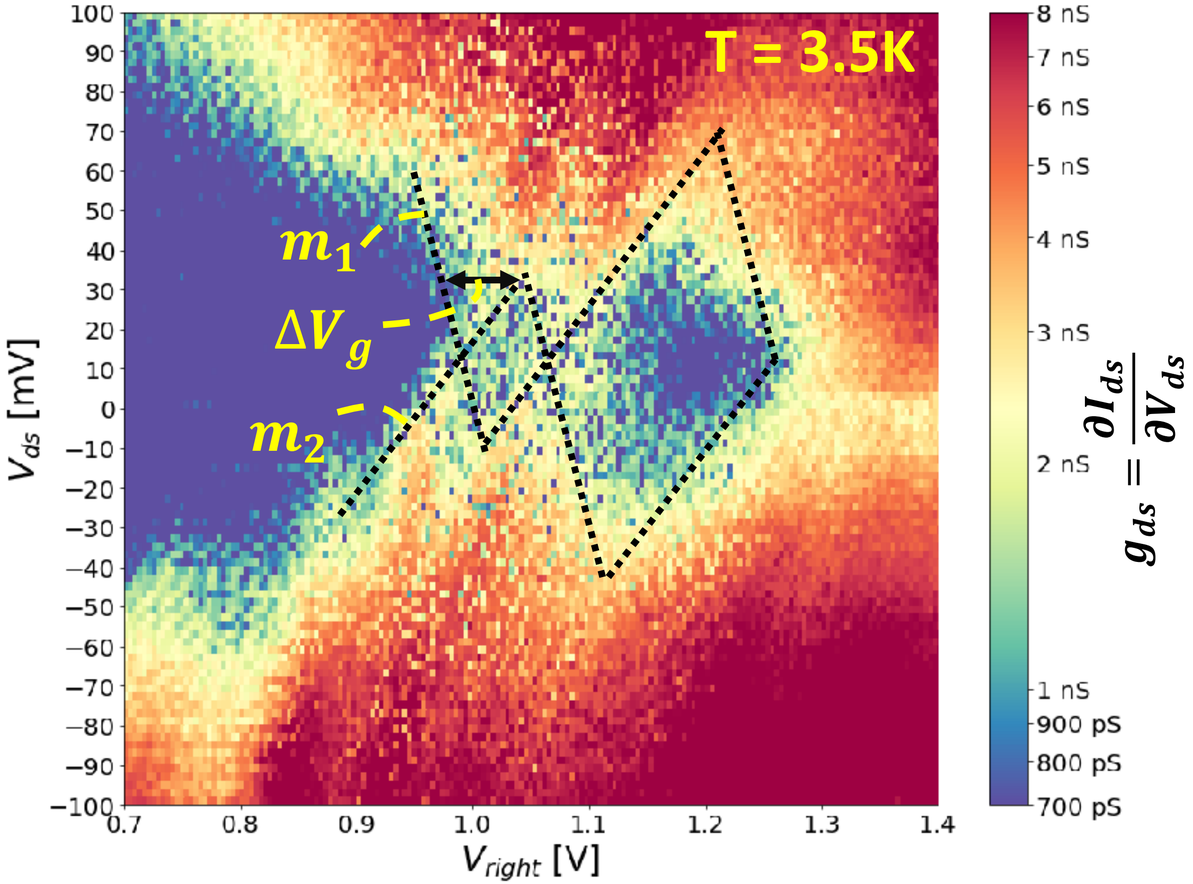
$$\Delta V_g = 150mV$$

$$C_g = \frac{e}{\Delta V_g} = 1.1aF$$

$$m_1 = \frac{-C_g}{C_i} \rightarrow C_s = 1aF$$

$$m_2 = \frac{C_g}{C_g + C_{d/s}} \rightarrow C_{d/s} = 1.7aF$$

$$\alpha = \frac{\Delta V_{ds}}{\Delta V_{gs}} = 0.3\frac{eV}{V}$$



Quantum Dot Parameter Extraction:
T. Y. Yang, et. al, "Quantum Transport in 40-nm MOSFETs at Deep-Cryogenic Temperatures," in IEEE Electron Device Letters, vol. 41, no. 7, pp. 981-984, July 2020.

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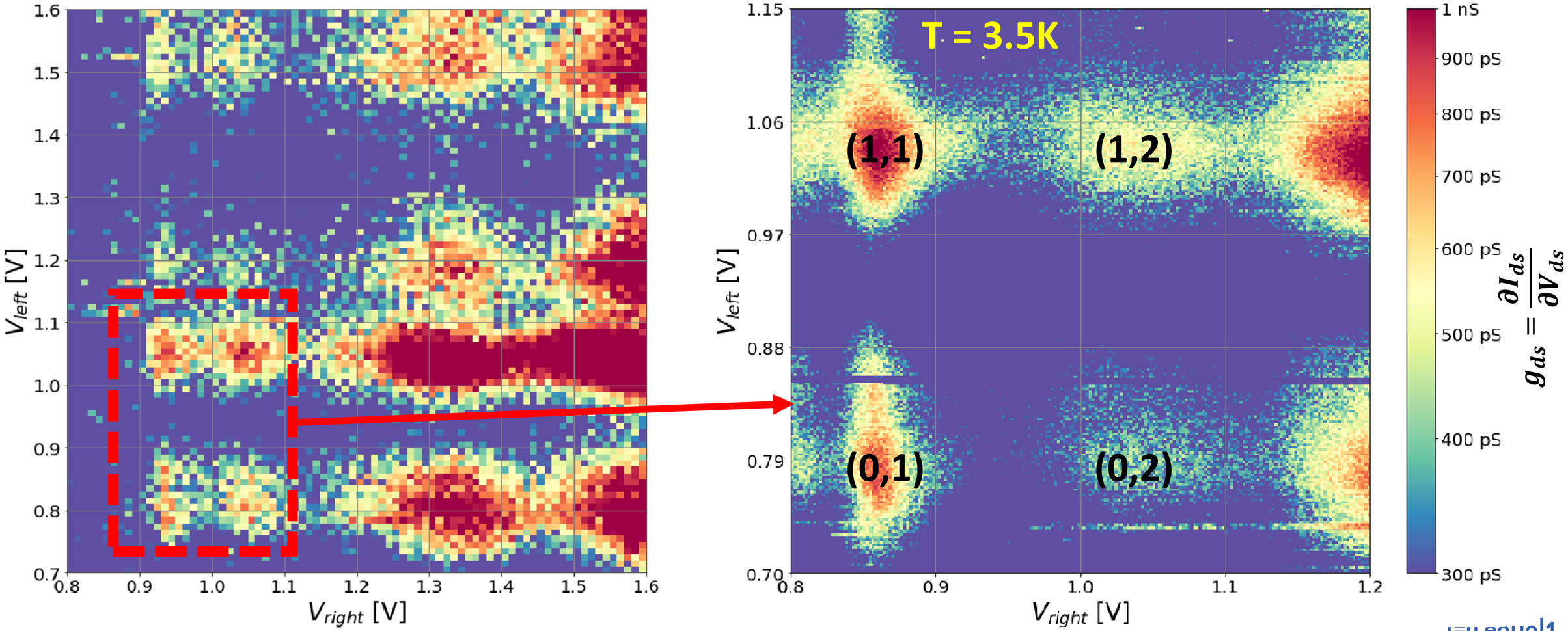
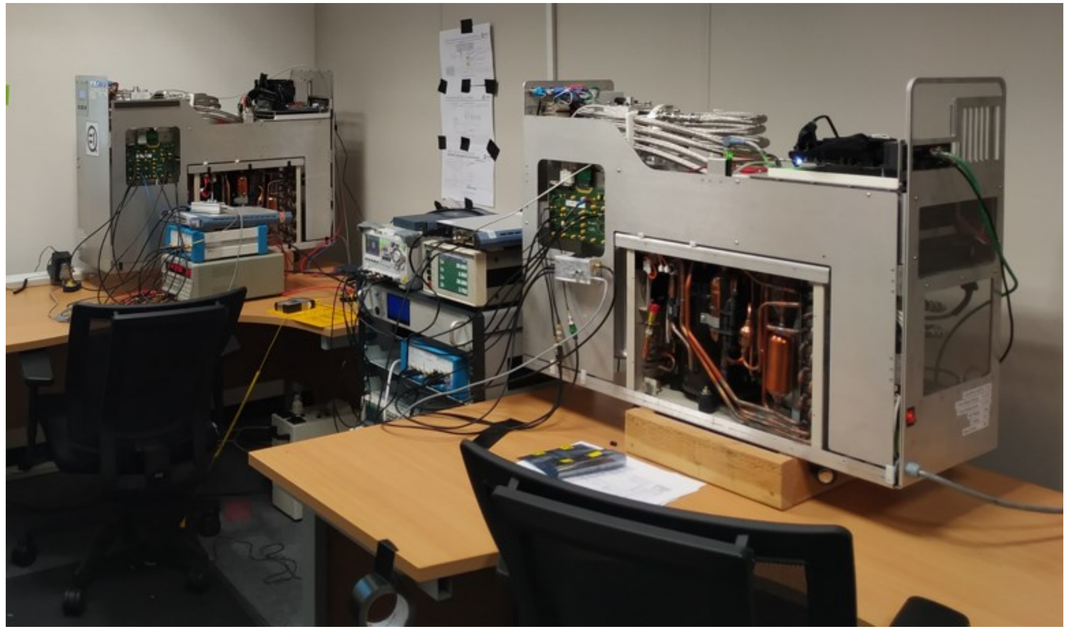
Measurement: charge stability (2)

Capability of loading quantum dots into triplet states



Conclusions

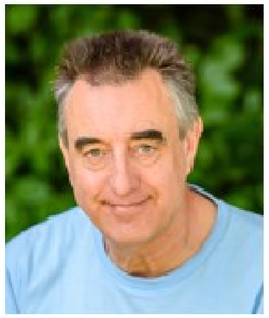
- Double well structure fabricated in 22-nm CMOS FD-SOI from GlobalFoundries
- Charge stability diagram measured → Capability to load electron using common mode back gate control
- Four (4) cryo-cooler operational at 3.3K (2 in San Carlos (USA) & 2 in Dublin Ireland)
- Spin resonance experiments on-going

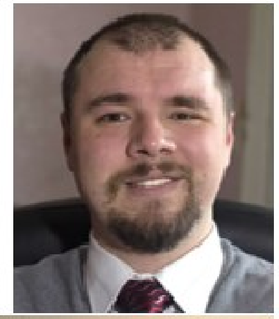


Acknowledgments




Calling all
Iron Warriors!

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